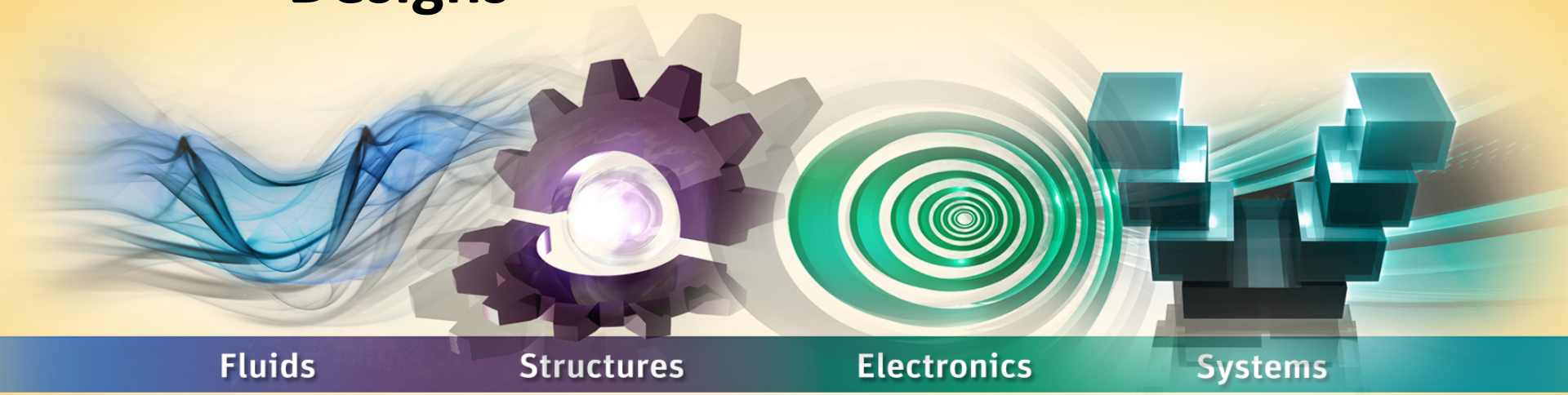
ANSYS

Realize Your Product Promise®

Achieving Thermal-aware EM through CPS Power-thermal Convergence in SoC/3D-IC Designs



Norman Chang
VP & Sr. Product Strategist, Apache BU

GSA, April, 2015

Technology Trends and Thermal Challenges

Higher Integration on 3D-IC

Thermal Interaction of Chips

Increasing Gate Density

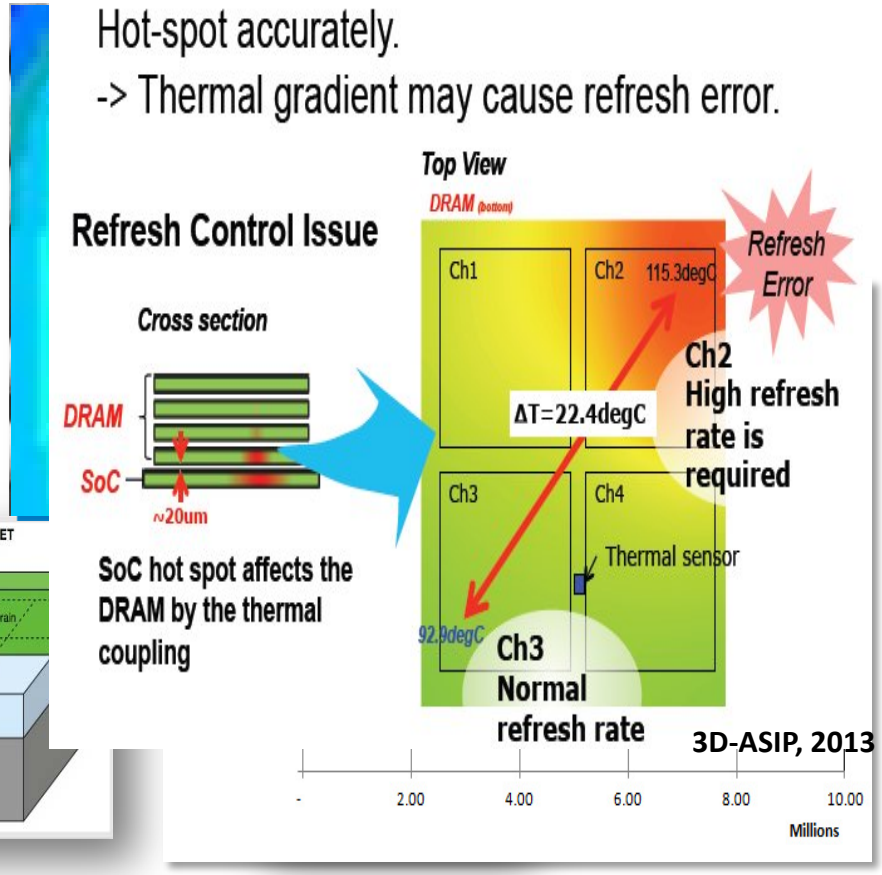
Elevated Thermal Impact

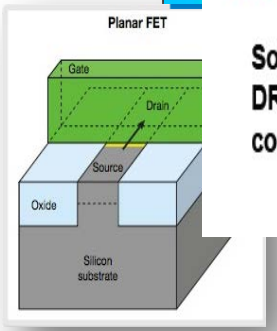
Higher Drive Strength Devices

Higher EM(T) Impact

Shift from Planar to FinFET

- Thermal sensor in DRAM cannot monitor the Hot-spot accurately.
  -> Thermal gradient may cause refresh error.

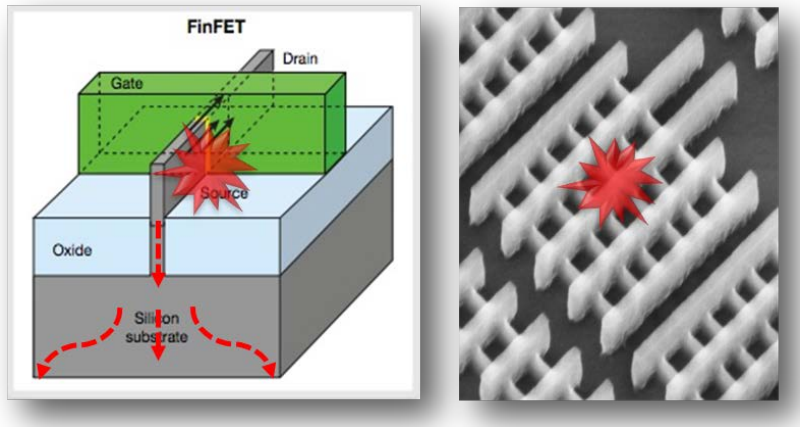




65nm 40nm 28nm **20nm** **16nm**

Impact of Self-heating on FinFET

- **Higher temperature on FinFET expected**
  - **Max. Temp increases with smaller Lg or larger Fin height**
  - **Narrow 3D fin structure and lower thermal conductivity of substrate create heat trap**
- **25C increase on FinFET degrades expected lifetime of device and metal layers by 3x to 5x**
- **How to estimate temperature rises?**
  - **FEOL (devices), BEOL (wires), and their thermal couplings**



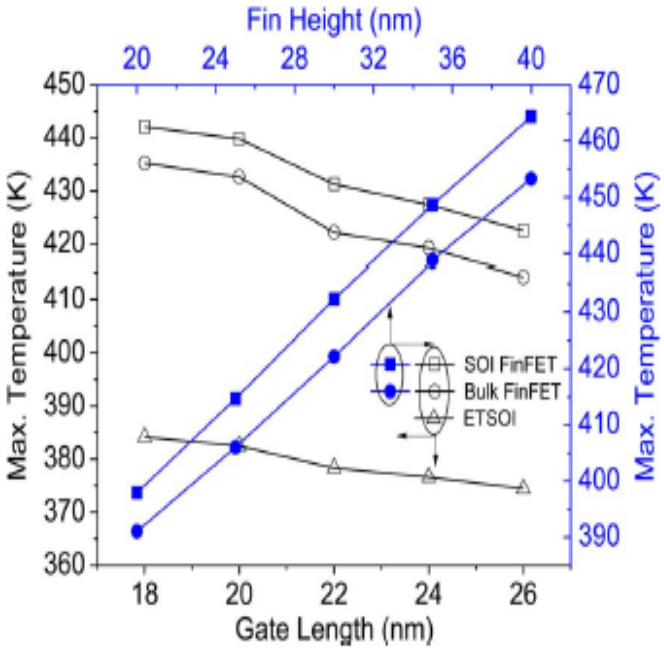
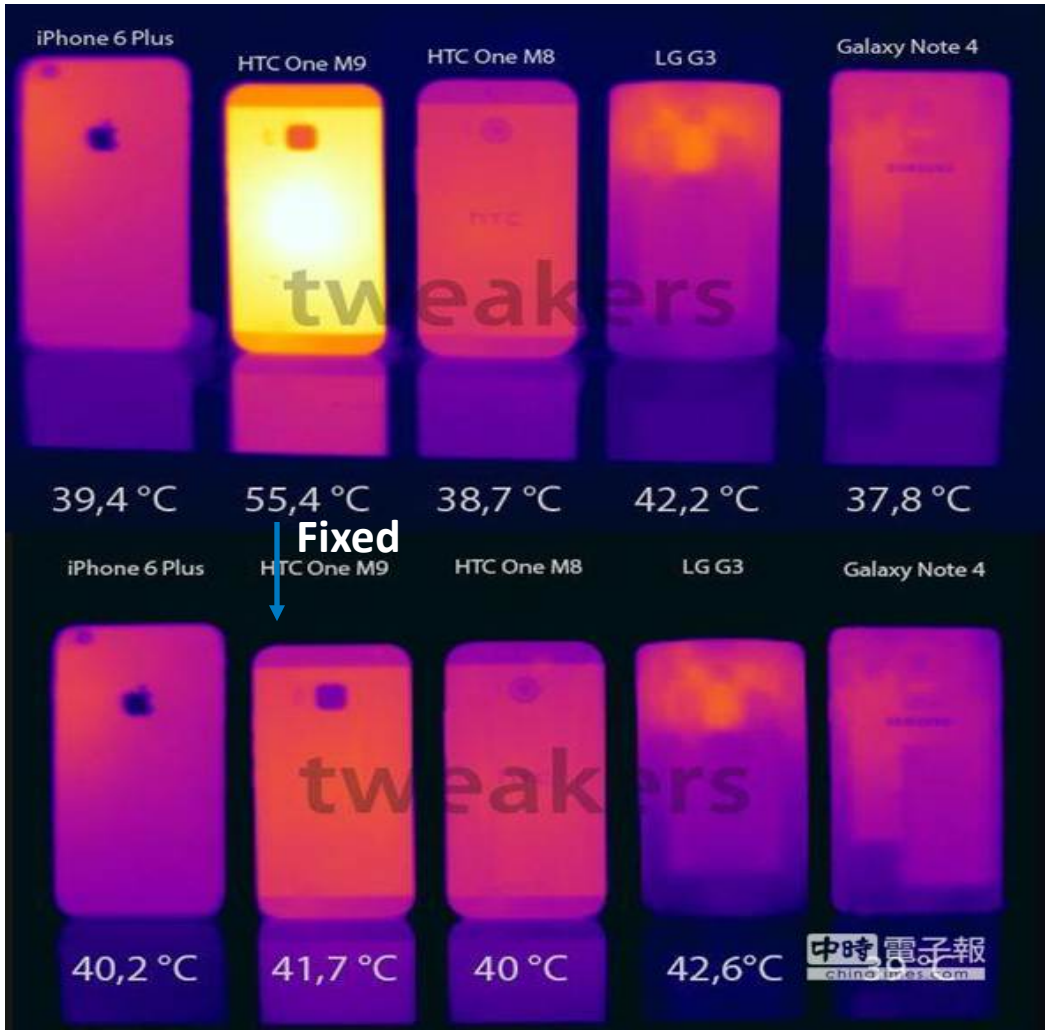


Fig. 8. Impact of scaling gate length and fin height on the self-heating behavior. The figure shows the following: 1) ETSOI device has a smaller temperature rise as compared to FinFET device, and 2) fin height scaling in FinFET device (similar to active area scaling of ETSOI) and gate length scaling can counterbalance the self-heating effect.

SHRIVASTAVA *et al.*: INSIGHT TOWARD HEAT TRANSPORT AND MODELING FRAMEWORK, IEEE TRANSACTIONS ON ELECTRON DEVICES, 2012

Overheating of Smartphones

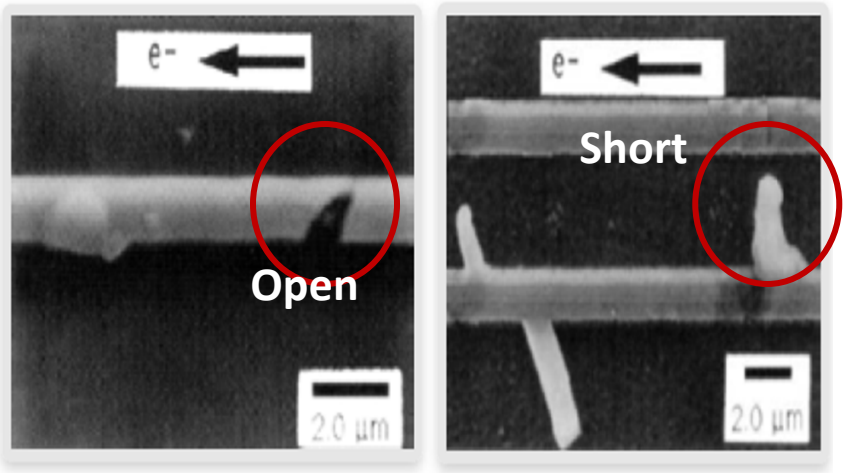


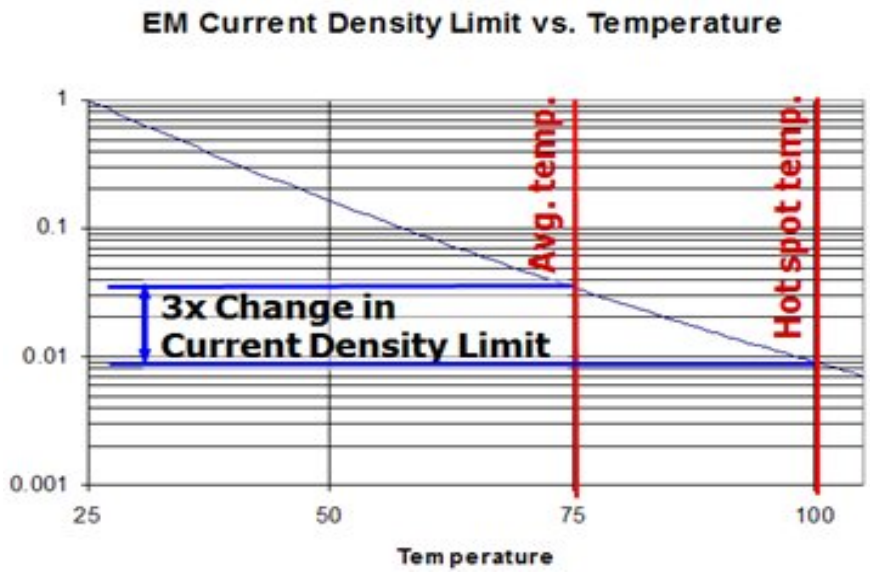
http://tweakers.net/nieuws/102040/htc-verhelpt-hitteprobleem-one-m9-met.html

- Overheating (> 45 degree C is uncomfortable Temp for humans) of mobile devices due to increasing integration of functions on SoCs
- Higher concentration of power and thermal hot-spot
- Thermal-aware EM on hot interconnect cluster need to be checked

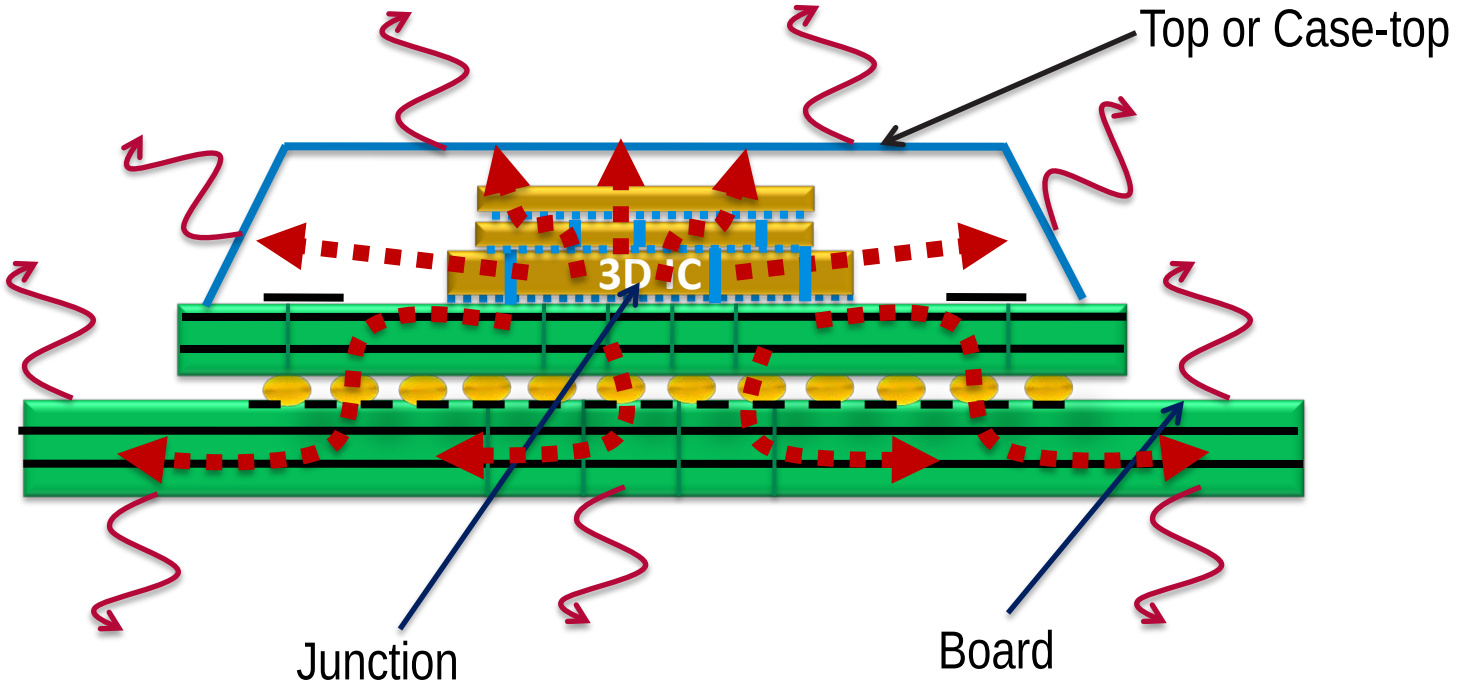
Thermal Reliability

- EM (Electromigration) is the gradual displacement of metal atoms due to high current density
  - Causing Open/Short circuits with void nucleation as a major threat
- High temperature (T) accelerates EM, a thermal reliability issue
  - Limiting allowable current density and lifetime degradation
- On-chip Tmax control and thermal run-away avoidance





Thermal Flow Path of IC-Package-System



Heat flow in 3D IC/package/board (conduction)

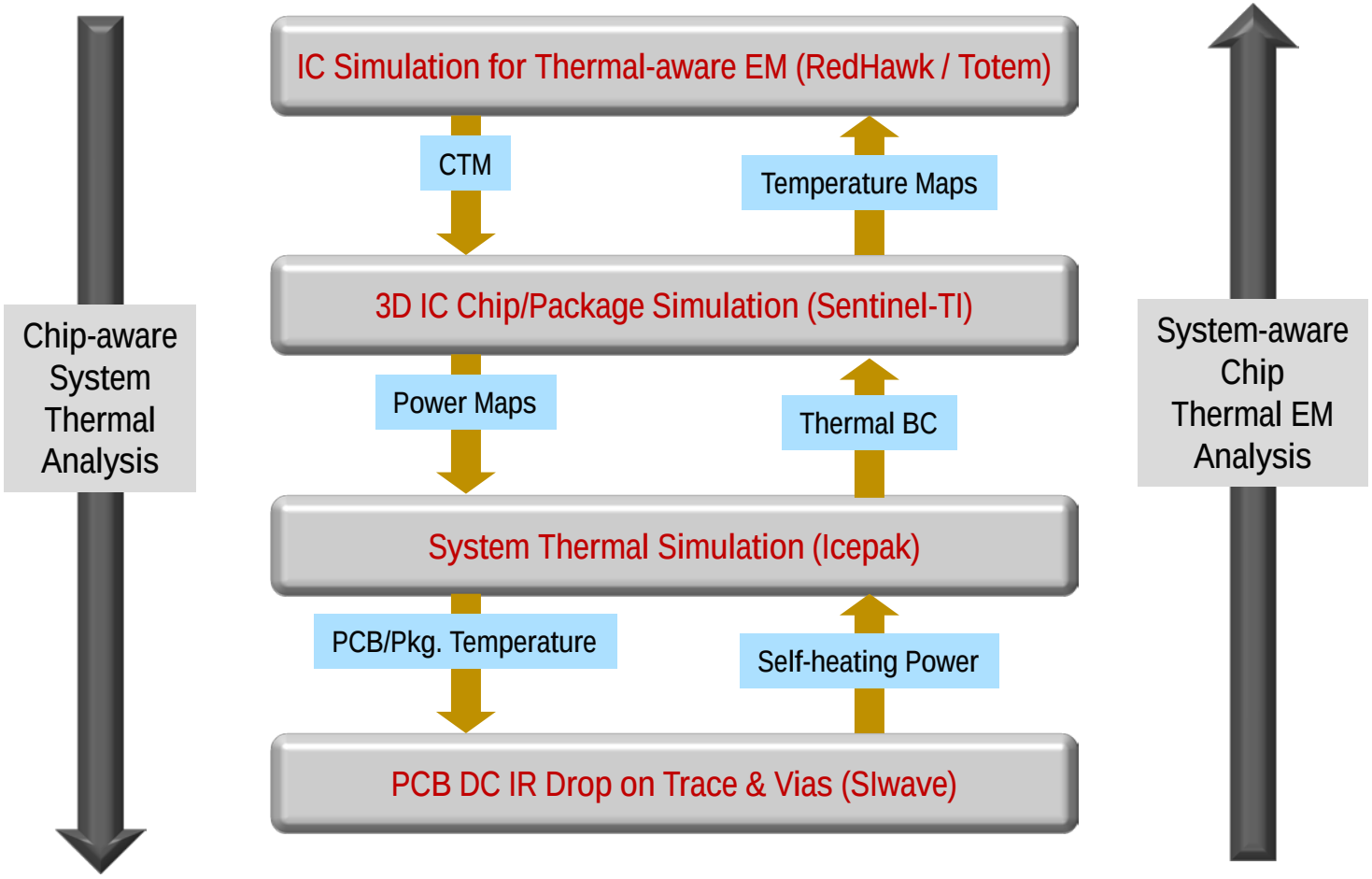
Heat dissipation from exterior surface (convection and radiation)

Equilibrium of Heat Flow

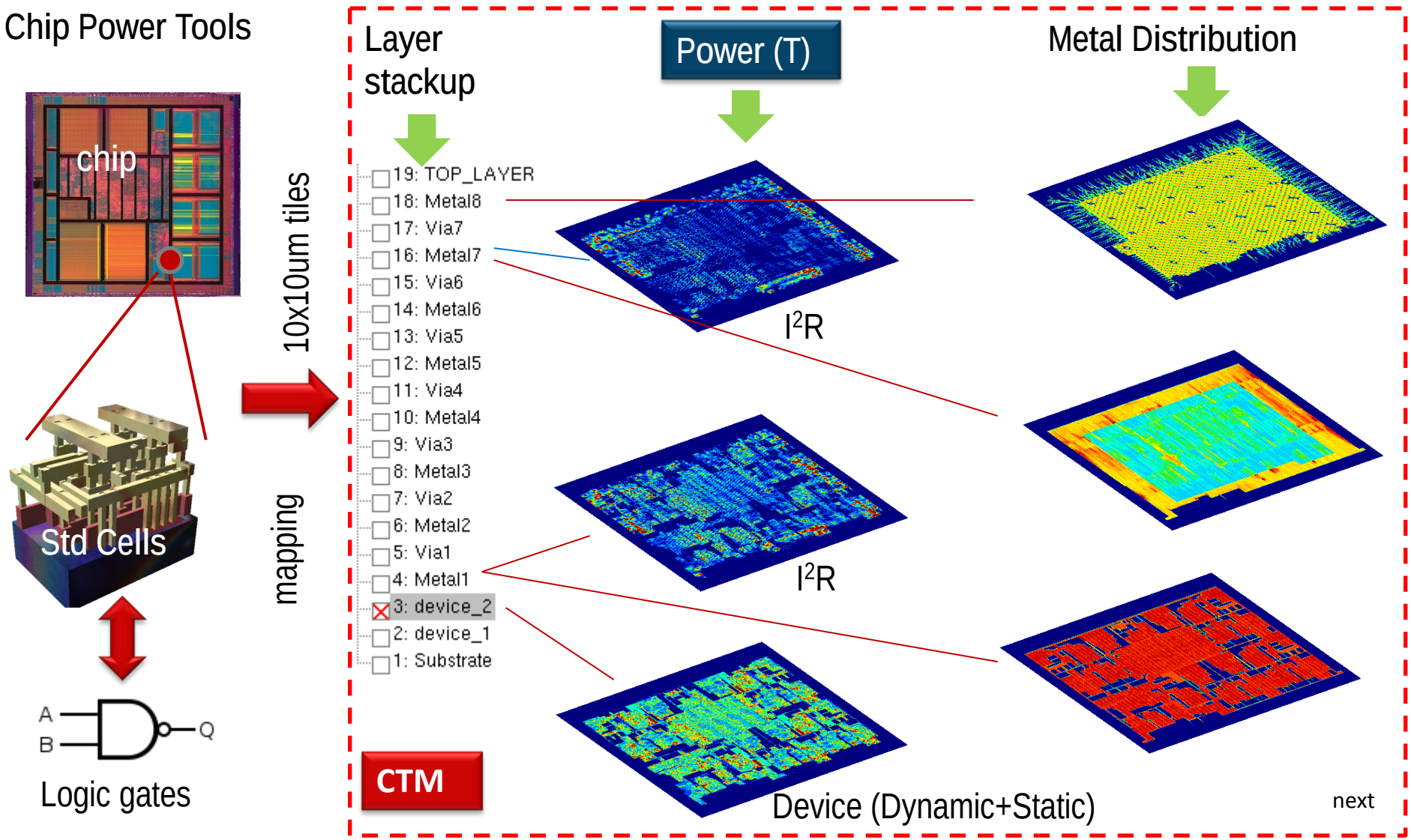
3D-IC and Package details are crucial for accurate on-chip thermal prediction

Chip-aware System Thermal Integrity

Chip-Package-System Thermal Co-analysis

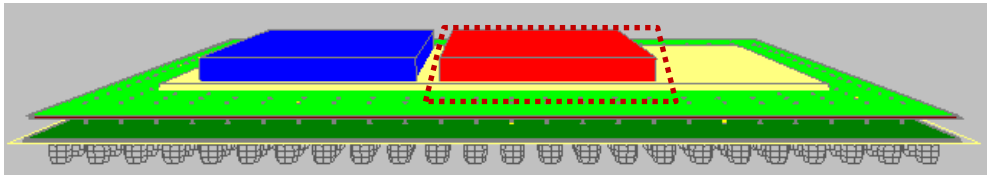


ANSYS Chip Thermal Model (CTM)

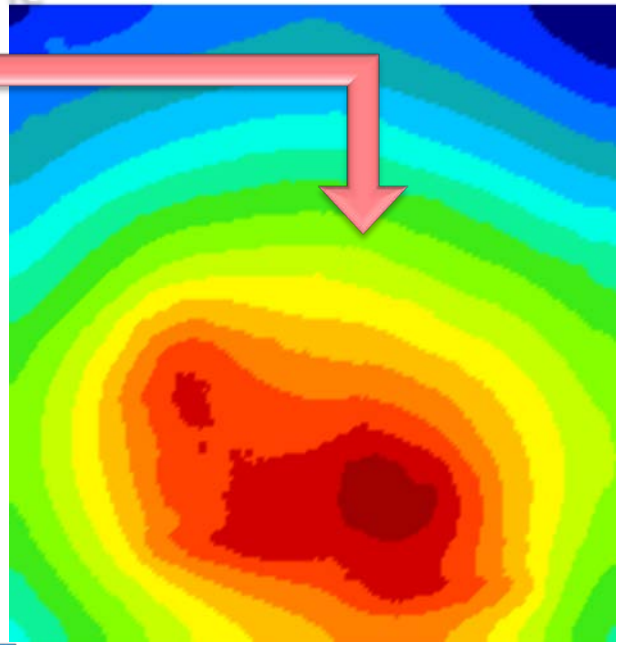


Power and Temperature Convergence Loops

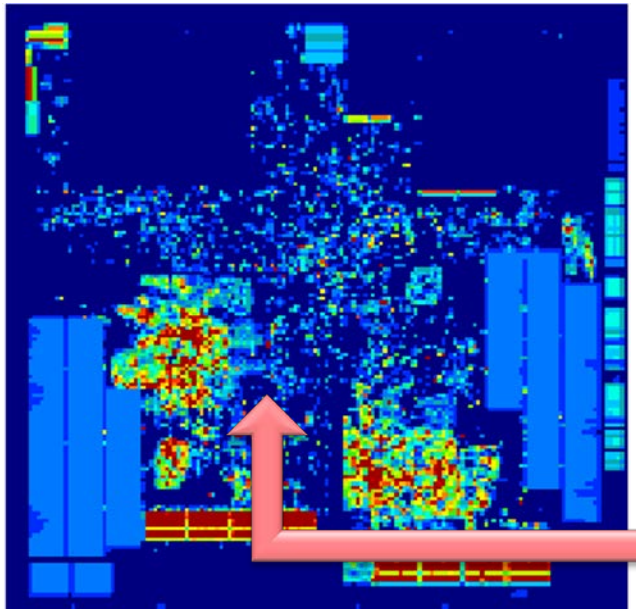
3D IC Model



Updated Temperature in 3D IC



Automatic on-chip power-temperature iterations for converged solution



Updated Power in 3D IC

CTM for each chip in 3D IC : Lookup power map from temperature map

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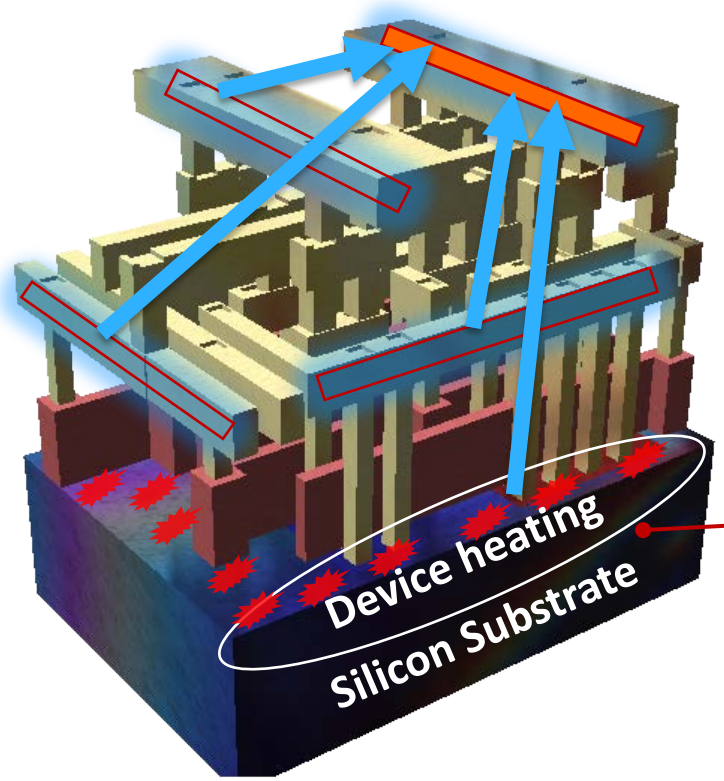
Instance/Device Layer and BEOL Thermal Analysis

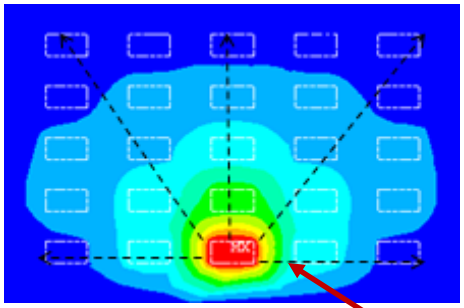
$$Wire\ \Delta T_i = \sum \Delta T_{ij}$$ **from both FEOL and BEOL self-heating**

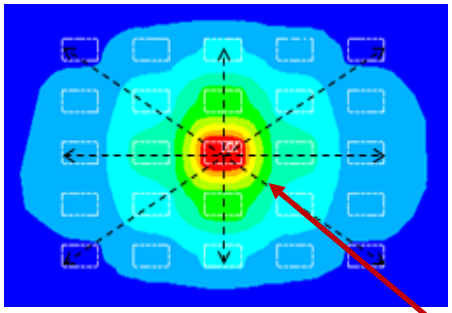


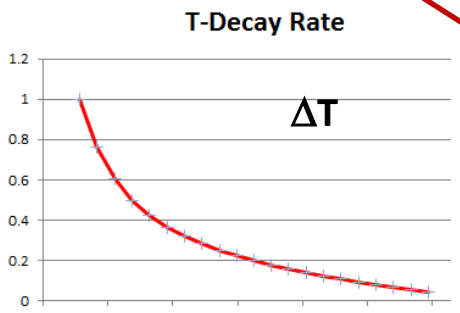
BEOL wire Delta-T due to selfheat-induced and thermal coupling among wires

Inst/Device Layer Thermal Analysis
CMOS, PMIC, photonic, RFIC, BJT with CTM-based thermal analysis

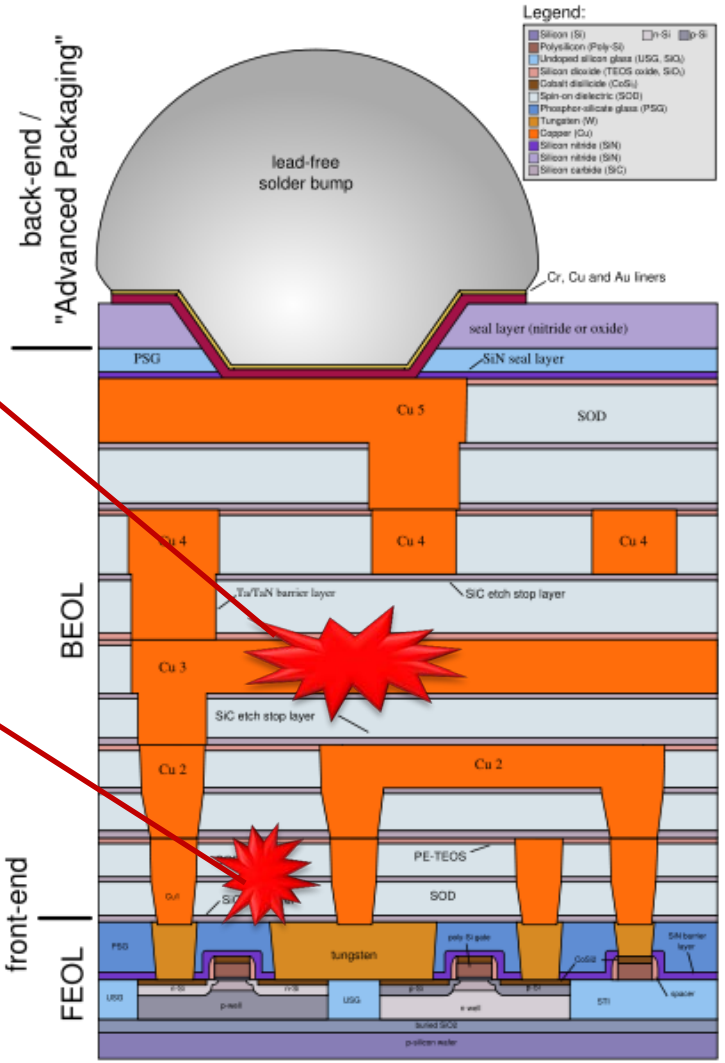
Fast Thermal Coupling Calculation for BEOL





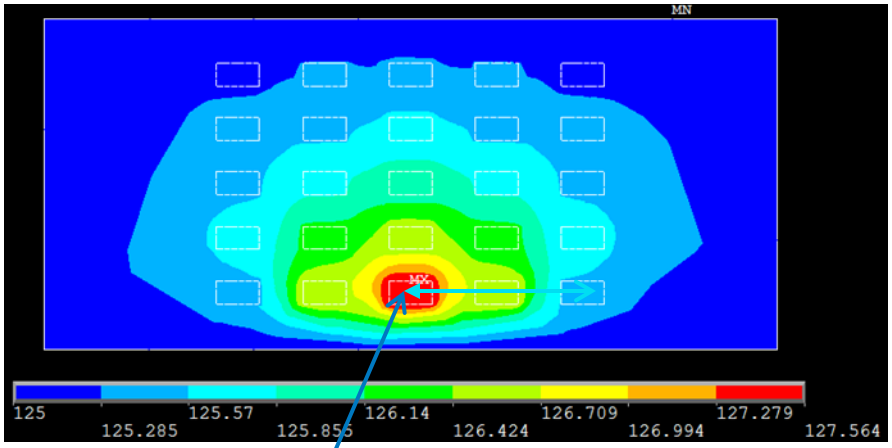


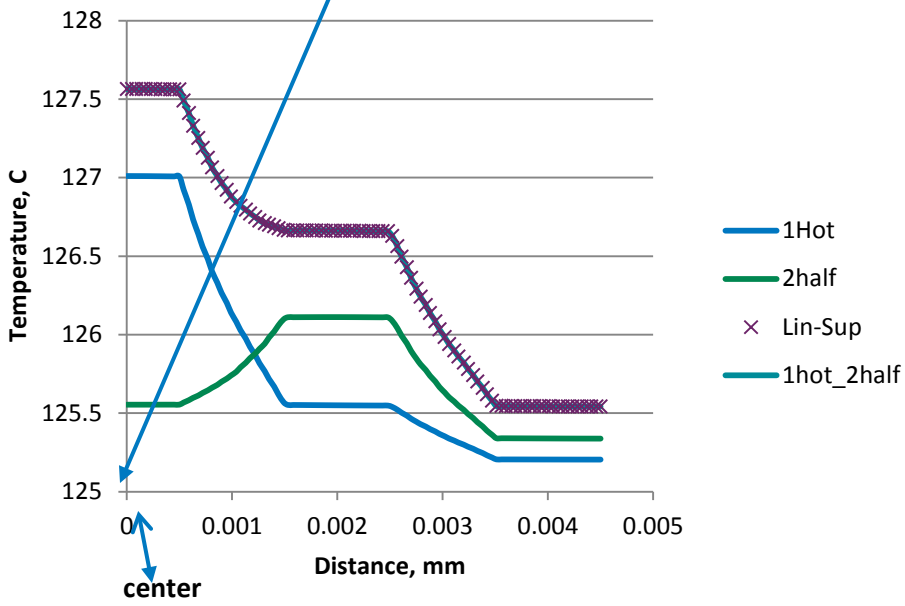
Thermal Coupling among Wires



- **Generate pre-characterized table of ΔT vs. distance**
- **With each wire and its neighbors, calculate total ΔT due to selfheat-induced and thermal couplings**
- **Combined with CTM flow for final wire Temp**

Correlation to FEM with Fast Thermal Coupling Calculation in BEOL

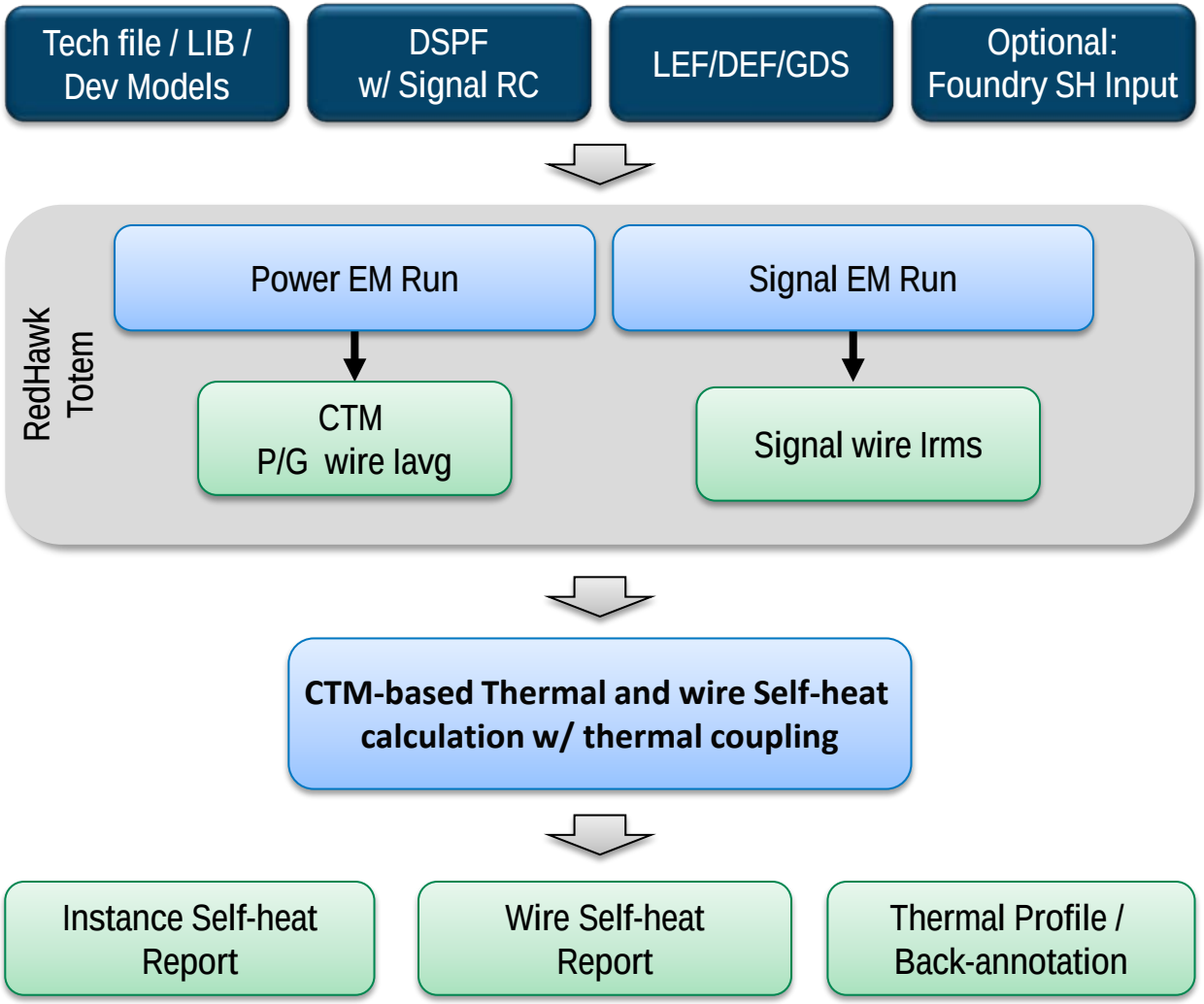




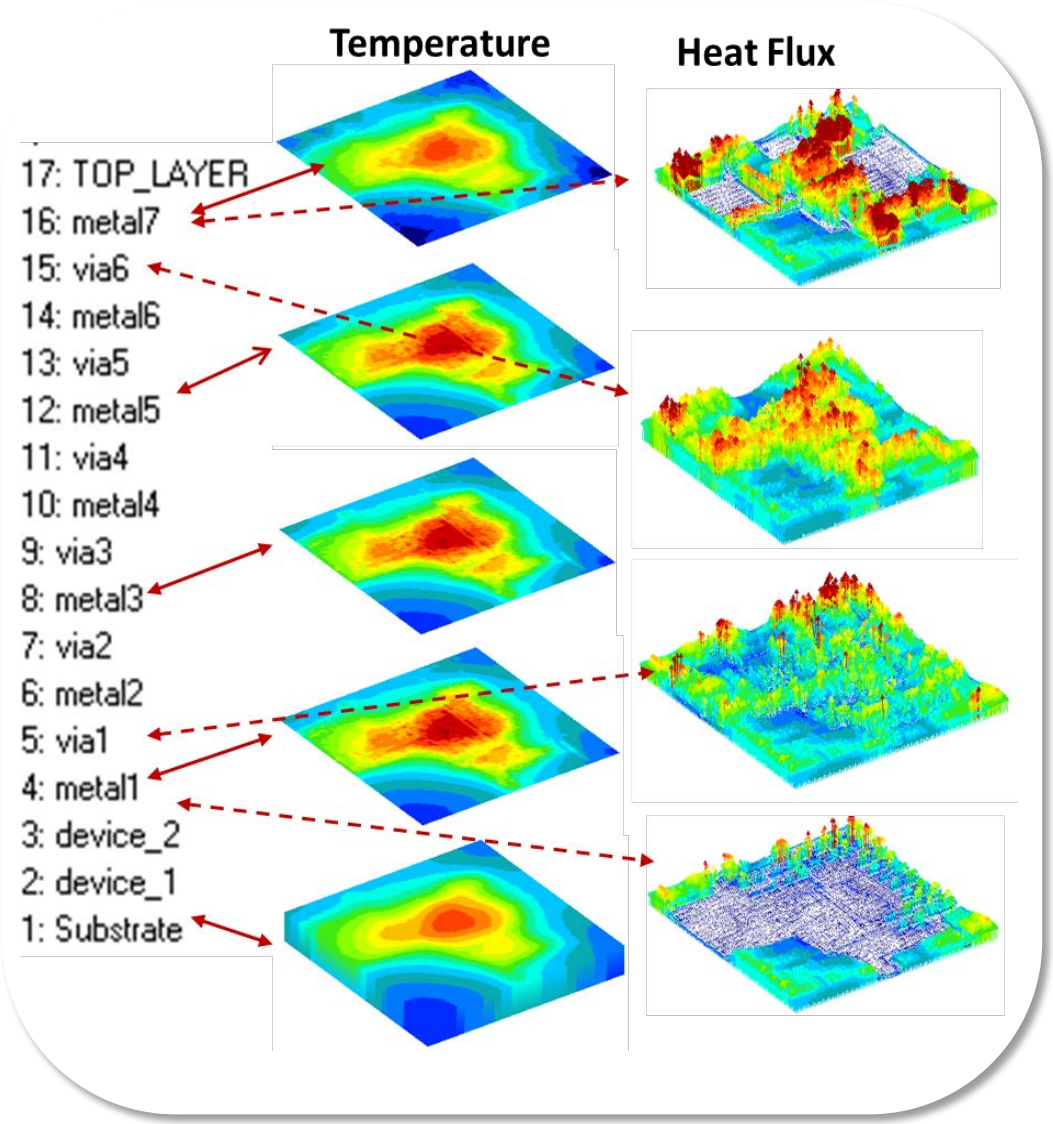
Exact matches for #3 and #4 in Temperature distribution ➔ Accuracy of Lin-Sup verified.

1. **1Hot: 1x pwr on center wire only (FEM)**
2. **2half: 0.5x pwr on side wires only (FEM)**
3. **Lin-Sup: (T1-125)+(T2-125)+125**
4. **1hot_2half: 1x+0.5x+0.5x pwr (FEM)**

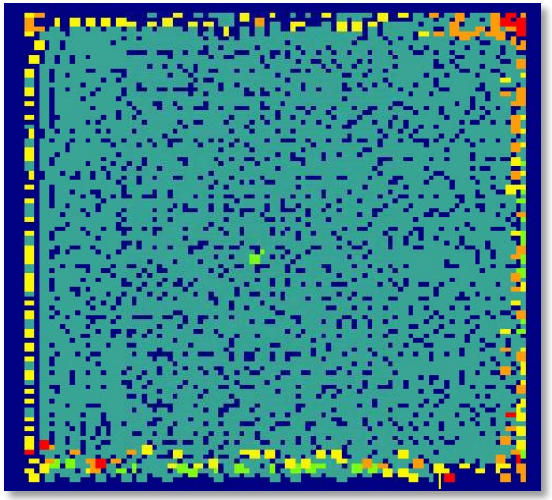
Self-heat Calculation Flow in RedHawk/Totem



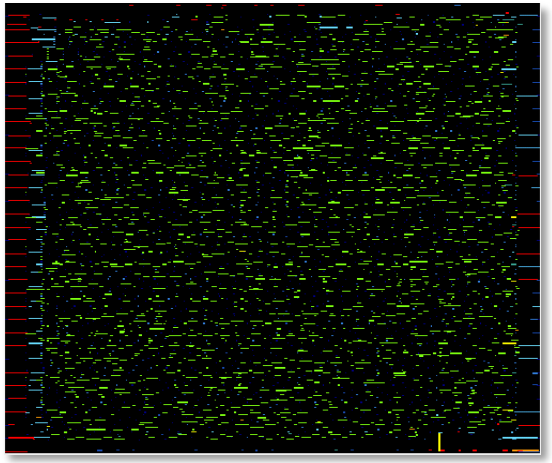
Example Metal Layer Temperature and EM Maps



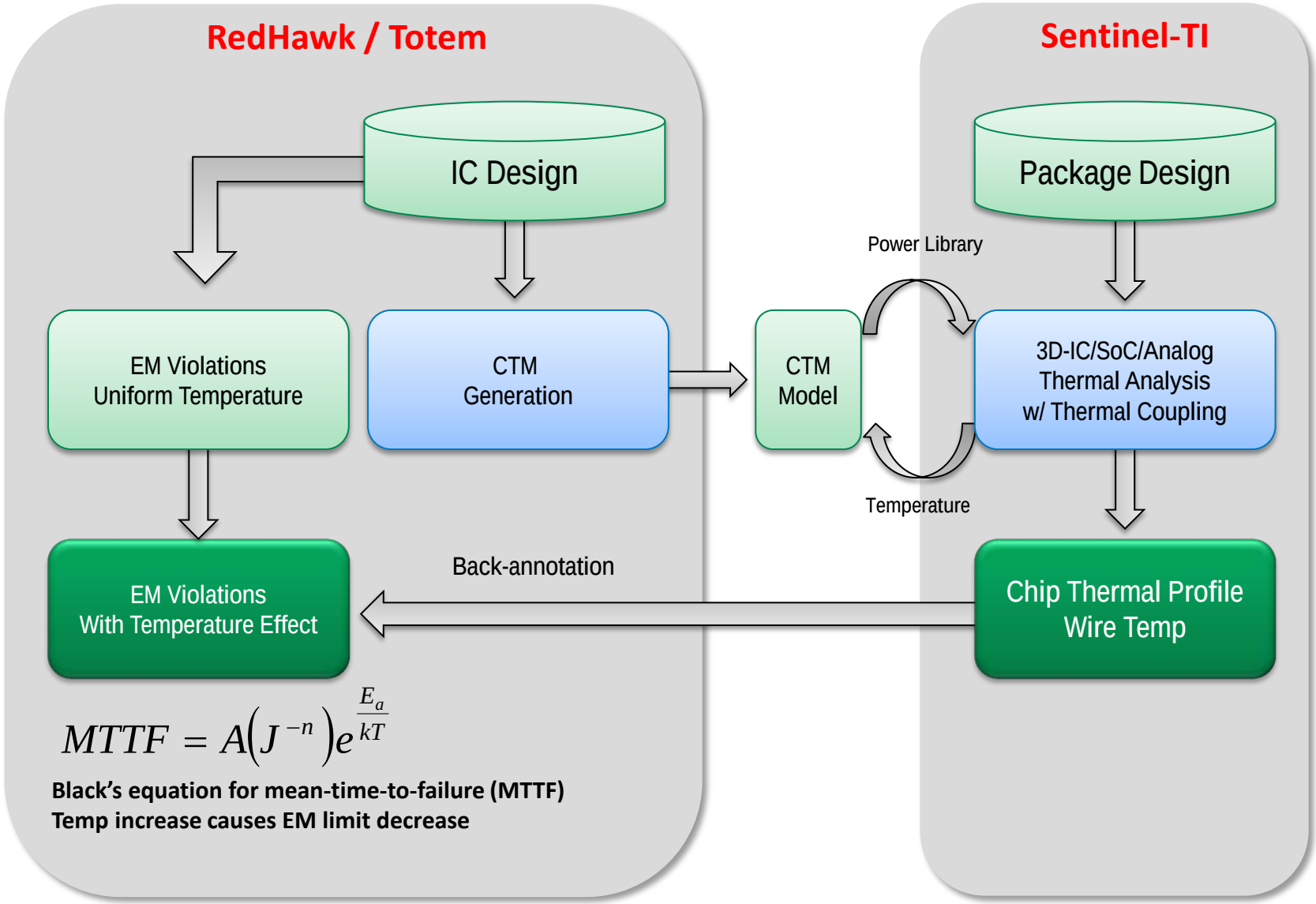
M2 Temp Map



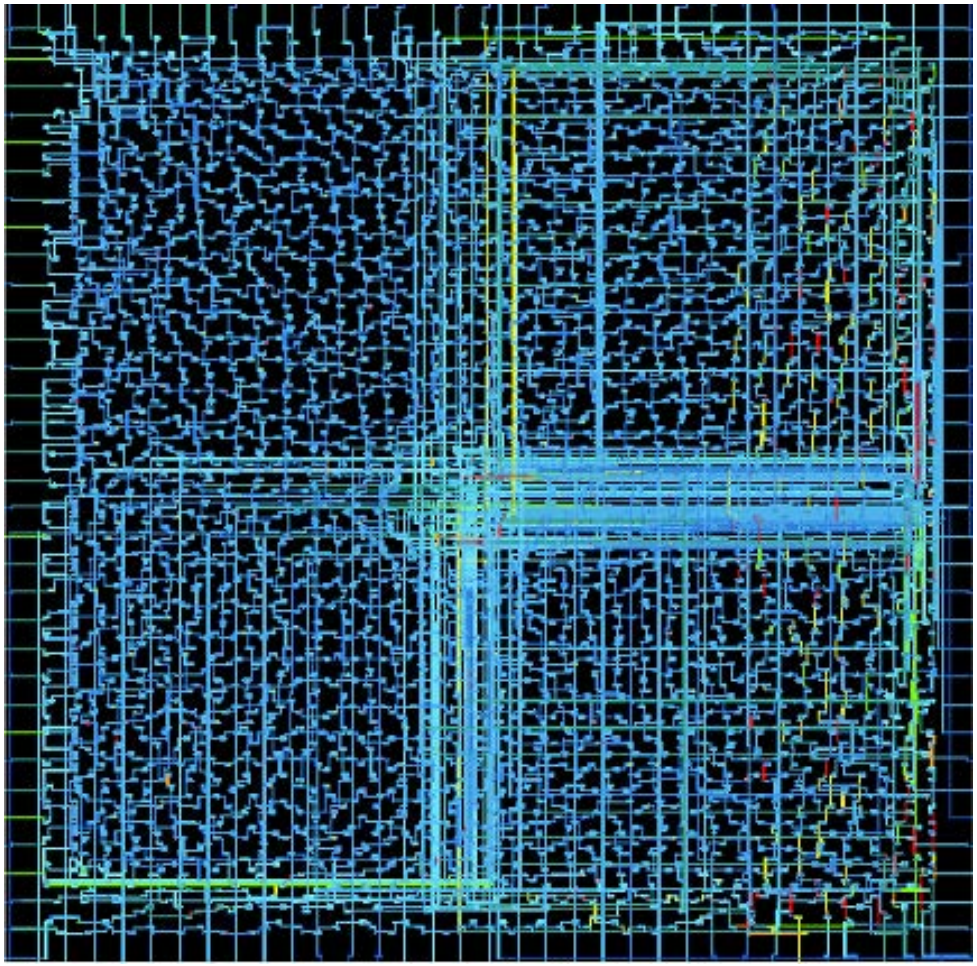
Signal EM (M2) Map



On-chip Thermal-Aware EM Flow

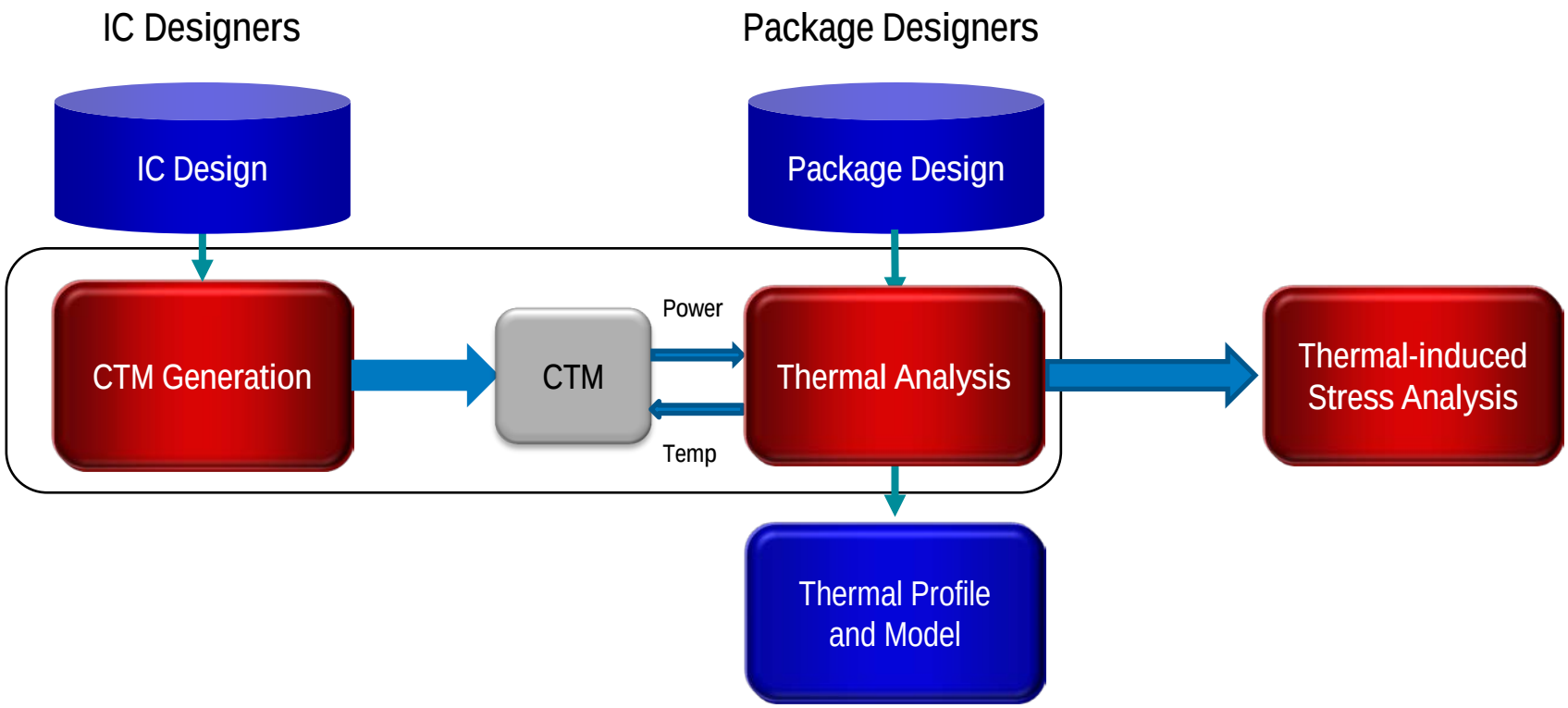


Thermal-aware EM Check with Wire Temperature Back-annotation on/ RedHawk and Totem



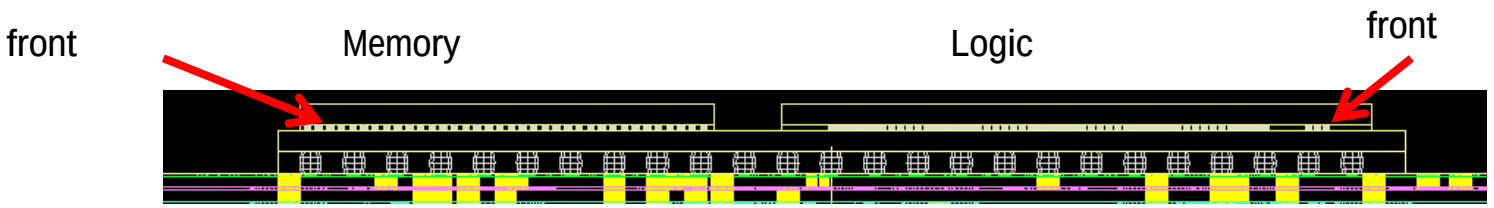
- Import wire temperature profile
- Update R and perform emcheck
- Show wire temperature and updated R, EM limit, and EM violation percentage

Chip-Package Thermal Stress Analysis

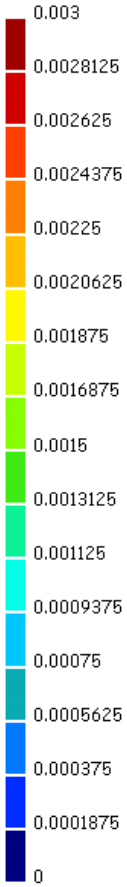


- **Temperature rise due to heating of chips cause differential thermal expansion**
- **Silicon chips have very low thermal expansion coefficients (2.6 ppm/C) and are push/pulled by surrounding components (> 12 ppm/C)**

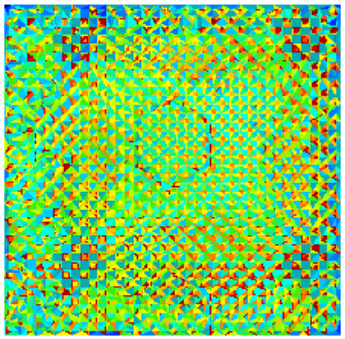
Front Face Stress of Memory and Logic



Courtesy of TSMC Ref. Flow

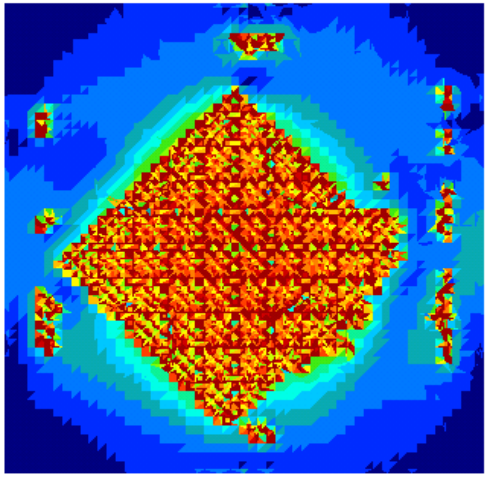


Unit = GPa



Tmax= 55.95 C

Tmax= 58.70 C

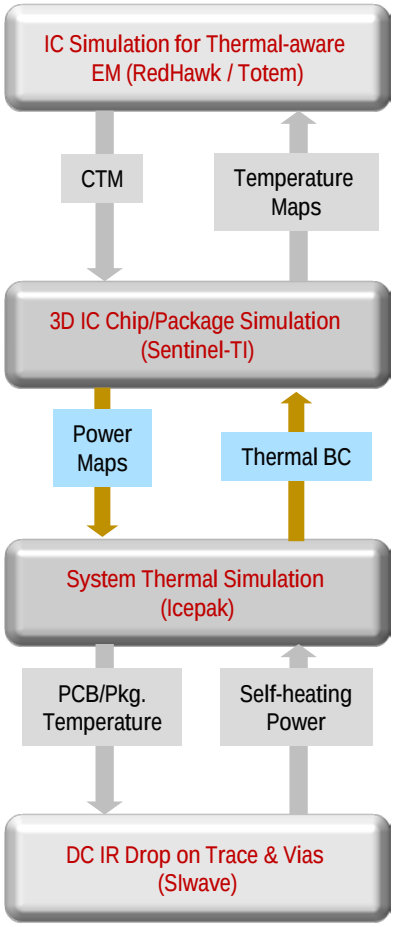


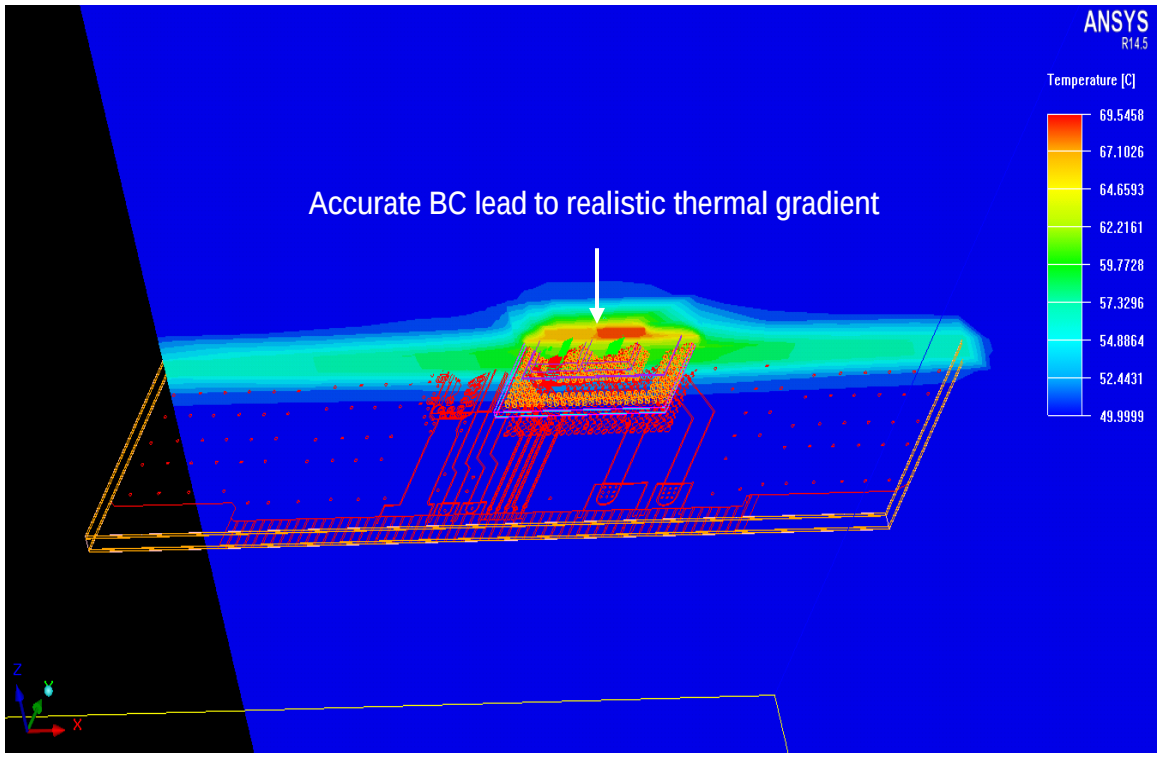
Viewed from bottom

Equivalent Stress

CENTROID STRESS-VM

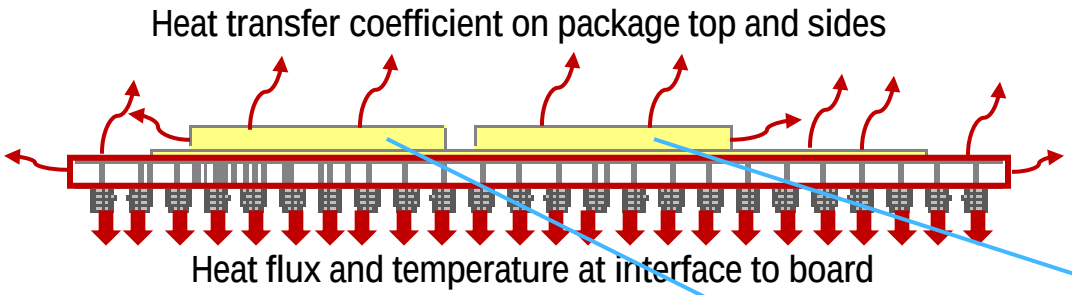
Realistic Thermal Gradient of Chips using System Thermal Analysis





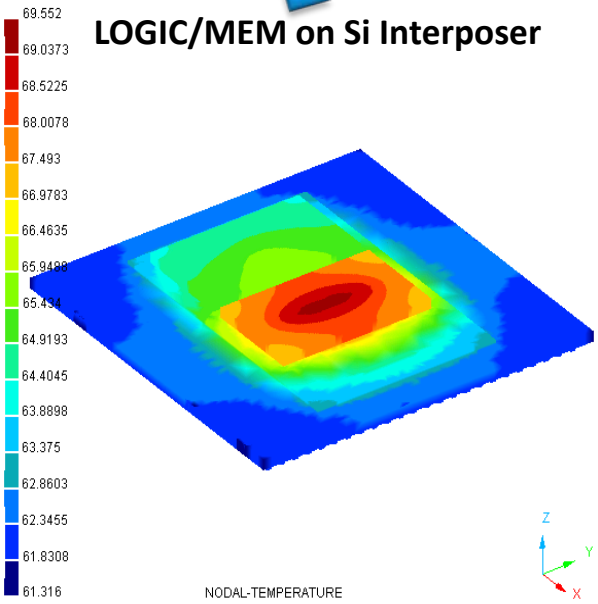
Computational Fluid Dynamics (CFD) simulation (using Icepak) of package in system with CTM-based power density map from Sentinel-TI to achieve the proper thermal boundary condition (BC) in chip thermal analysis.

Converged Thermal Profiles of Chips

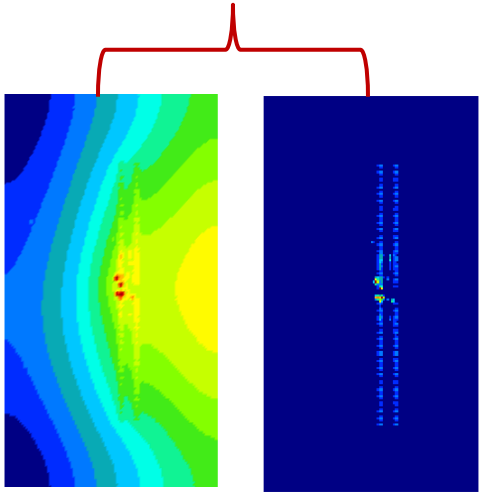


Accurate system thermal boundary condition from Icepak CFD simulation

LOGIC/MEM on Si Interposer



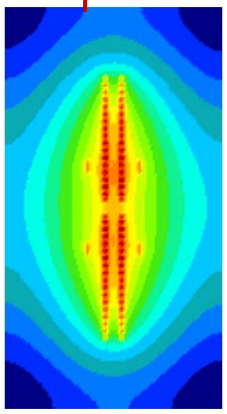
LOGIC



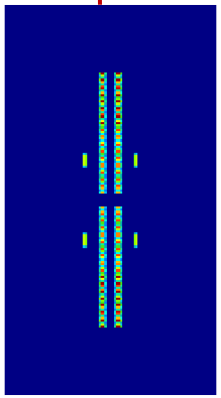
Temperature

Power Density
(~ 0.20W)

MEM



Temperature

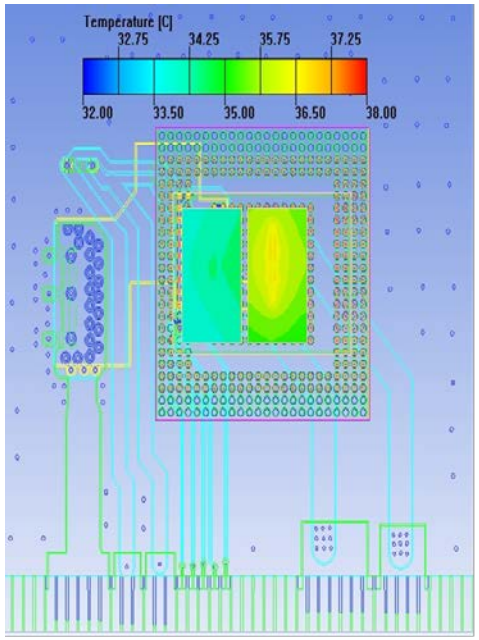


Power Density
(~ 0.87W)

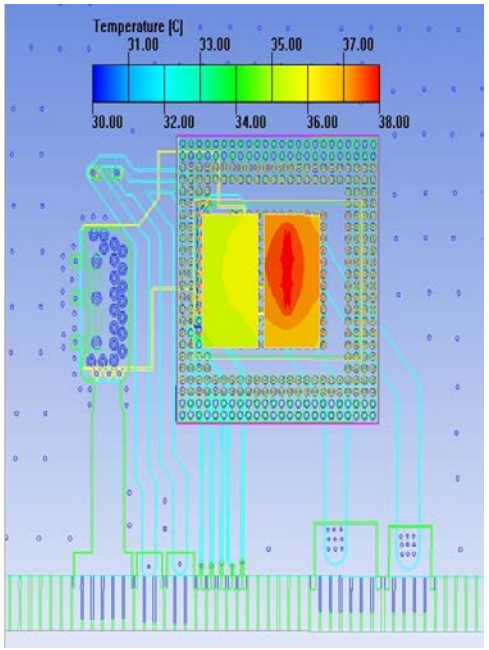
PCB Temperature Profile with Joule Heating Based on C4 Bump Current from CPM

- C4 bump current from CPM (Chip Power Model) generated by RedHawk imported to SIwave
- Simulated: Forced convection JEDEC chamber with flow velocity = 1 m/s
- System ambient temperature = 20ºC
- Wire temperature rise of 1.5 ºC (7.5% increase) with self-heating

No PCB Joule Heating



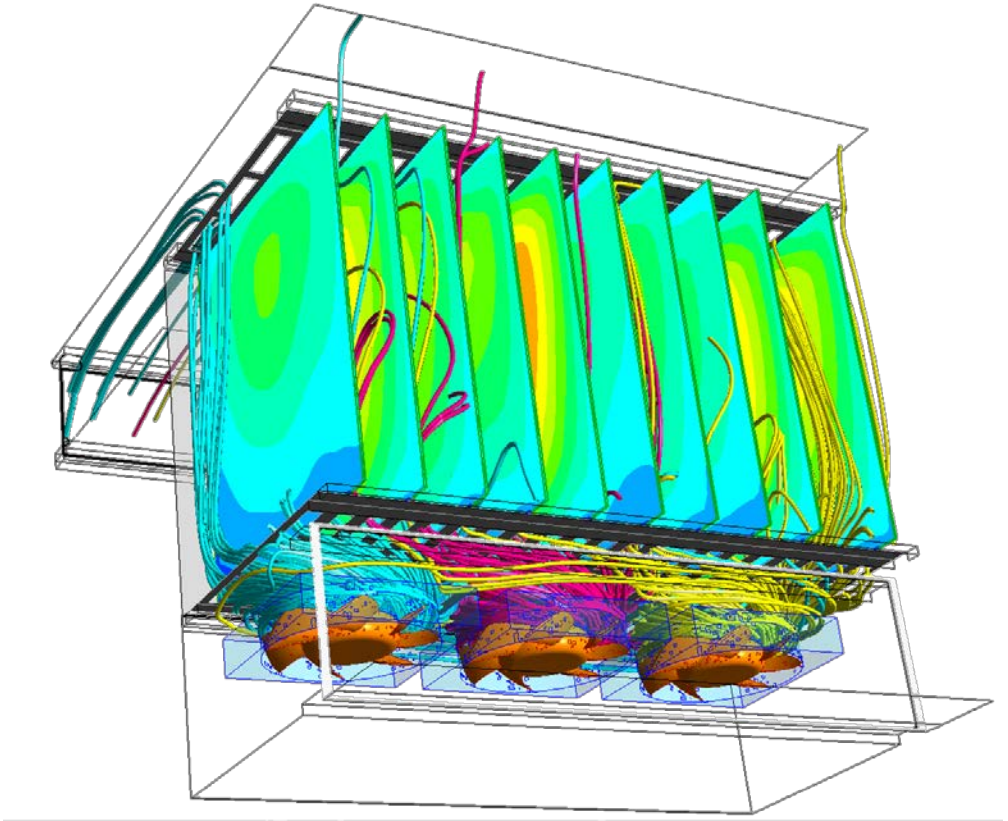
With PCB Joule Heating



ANSYS Icepak for Electronics Thermal Management

ANSYS Icepak is an integrated electronics cooling solution for IC packages, printed circuit boards and complete electronic systems

- Fluid flow (Laminar and Turbulent)
- Conjugate heat transfer
  - Conduction
  - Convection (Natural and Forced)
  - Radiation (Thermal and Solar)
  - Joule Heating
- Steady state and transient thermal analysis
- Single or multiple fluids
- Species transport



Velocity streamlines and temperature contours for a card array in a VME format box cooled by three axial fans modeled using a moving reference frame (MRF) fan model

Key to Chip-Package-System Reliability and Robustness – Thermal Integrity