ANSYS

White Paper

Package on Board Simulation with 3-D Electromagnetic Simulation

For many years, designers have taken into account the effect of package parasitics in simulation, from using simple first-order models, like ideal inductance + resistance, to more complex spice ladder networks and finally to full extraction of s-parameters of the package using 3-D electromagnetic simulators. For package plus PCB channels, currently the most common process is to extract the package and board independently as an s-parameter or broadband SPICE model and to combine both models in a circuit simulator. This approach has increasing limitations due to factors such as higher frequency of operation, increasing signal speed and more complex integrated devices.

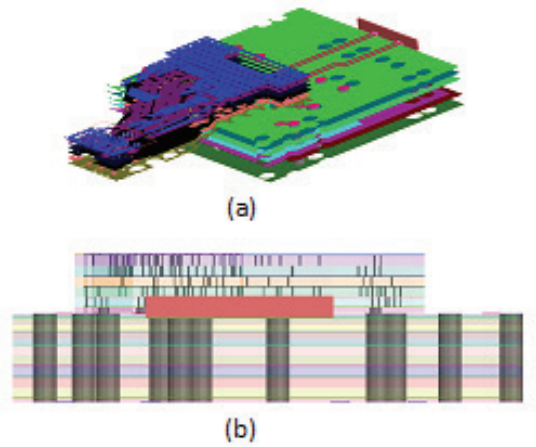

Figure 1. Package on board: (a) 3/4 view; (b) side view

The coupling between the package and the board (or package and circuit) has a significant impact on the performances that cannot be neglected. Achieving simulation of a complex package and board, or package and circuit has several challenges: capacity and accuracy of the electromagnetic solver, automation, ease of use, acceptable simulation time.

Board and package designers know how important it is to extract an accurate model of their design when included in higher-level system simulation. Using 3-D full-wave electromagnetic simulation along with automatic adaptive meshing schemes provides the accuracy level needed for extracting full wave s-parameter models. Nevertheless, designers face several challenges when trying to use 3-D EM simulation to address complex designs, like the example shown in Figure 1. Usually board and package devices are designed with electronic design automation (EDA) tools and need to be imported into the 3-D electromagnetic simulation tool. These designs include several dielectric layers, power and ground planes, signal layers, large number of vias (associated with padstack definition) and bondwires. The first challenge is to import the database from the EDA tool excluding manual modification to be applied to the design but keeping database information for traces, padstack, bondwire, net and pin. Once the geometry is imported, additional simulation settings (for example, port definition) need to be user friendly, avoiding time-consuming engineering effort and providing accessibility for the non-expert user. Finally, the 3-D electromagnetic simulation tool requires powerful mesher, solver and high-

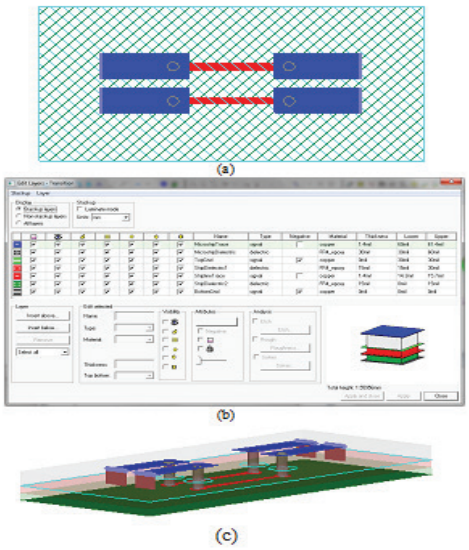

Figure 2. (a) 2-D drawing; (b) associated stack-up; (c) resultant 3-D layout

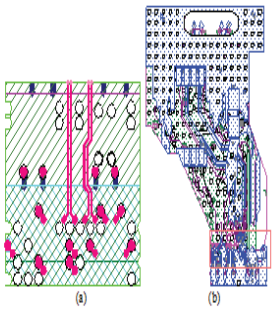

Figure 3. (a) Board cut-out; (b) package cut-out

performance computing features to shorten simulation time to an acceptable level — while at the same time providing accuracy. This paper details a new process for package on board 3-D electromagnetic simulation using ANSYS® HFSS™ 3-D layout.

Import Design

The first innovation is to provide an alternative interface for ANSYS HFSS, the gold standard tool for 3-D full wave electromagnetic simulation, accuracy and speed, which fits into a flow with layered structures and designs. The design entry is a 2-D layout with associated stack-up definition used to create a 3-D structure (Figure 2).

This interface is similar to the one used by board and package designers in a classic EDA flow. Full database design can be imported by reading *.brd, *.mcm, *.sip or ODB++. All information, drawing primitives, nets, padstack, bondwire and stack-up definitions are translated in the 3-D layout interface. Moreover, maintaining drawing primitives allows definition of parameters, such as trace width, that would not be possible with simple polygons. Once imported, a part of the layout can be cut out by selecting nets of interest or specifying an area using a polygon. The complete board was imported using *.brd file, then a cut-out design was created by selecting a few nets. The full package was imported using *.mcm file, then a cut-out design was created by selecting the nets of interest. Figure 3 shows the top view of both package and board. Notice that the package and the board do not have the same stack-up, which could be challenging if you want to combine the board and the package in one simulation. HFSS 3-D layout flow supports hierarchy, which means you can combine two designs that have different stack-ups with a simple copy/paste.

Figure 4 shows the 3-D view of the package, board and results of the copy/paste package on board design. The package on board design clearly shows that usage of finite dielectric is mandatory to correctly represent the physical structure, as the dielectric layer from the package must only be drawn where the package is located. The finite element method (FEM) used by the electromagnetic solver handles any arbitrary 3-D structure and finite dielectric layers.

Set Up Simulation

Once the design is imported, a few more steps are required before running the simulation. The first step is to define excitations. Thanks to significant automation, this step is as simple as selecting an edge or a via and converting it to a port (Figure 5). Once the ports are created, three more steps are required: Define simulation setup, frequency sweep and air box size. These are accomplished by entering parameters in the relevant properties window. The simulation setup defines the parameters used by the solver to create the initial mesh and to complete the automatic adaptive mesh process. Several options allow the user to optimize the setup with regard to the structure simulated. For this specific design, the solution frequency is

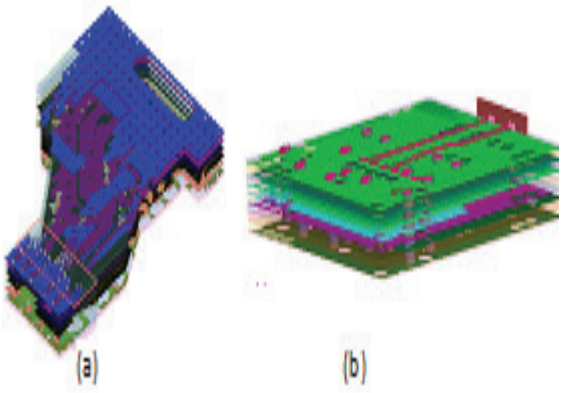

Figure 4. (a) Package design; (b) board design; (c) package on board after copy/paste

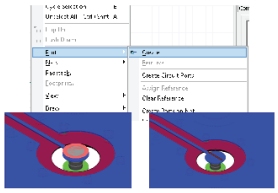

Figure 5. Automatic port creation

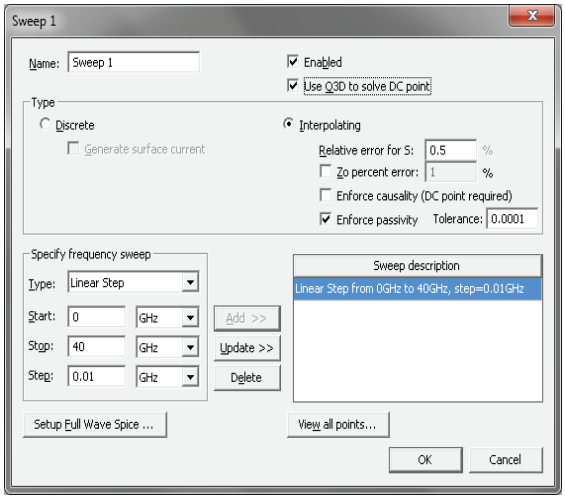

Figure 6. Frequency sweep properties window

set to 20 GHz (frequency used for adaptive process), since we want simulation results in 0 GHz to 40 GHz bandwidth. The order of basis function is set to mixed order and the iterative solver is selected. The frequency sweep setup is defined with regard to the final usage of the extracted model. In most cases, the extracted model is used in time domain circuit simulation combined with active models (drivers, receivers) to evaluate the impact of the package and board on the transmitted signal. For example, eye diagram performance can be evaluated. Even if the extracted model can be a broadband spice model, the default format is S-parameters.

The S-parameter file needs to verify specific time domain circuit simulation criteria:

- Accurate DC point
- Passivity
- Causality

The frequency sweep setup provides specific options with regard to these criteria (Figure 6). By checking the option “Use Q3D to solve DC point,” a quasi-static solver will be called to accurately compute the DC point. The user can select either a discrete sweep, for which all frequencies from the sweep will be simulated, or an interpolating sweep, in which an adaptive rational-function interpolation method is used to perform the sweep. For broadband simulation, the interpolating sweep is much faster than the discrete sweep but, in some cases, may result in non-passive or non-causal results. The user can choose to enforce passivity and to enforce causality for the interpolating sweep. Usually enforcing passivity is enough.

For this case, we used interpolating sweep and selected the option “Use Q3D to solve DC point” and “Enforce passivity.” Concerning the causality, a common reason for non-causal results is the use of material properties with no frequency dependence defined. For this simulation, we used frequency dependant material properties.

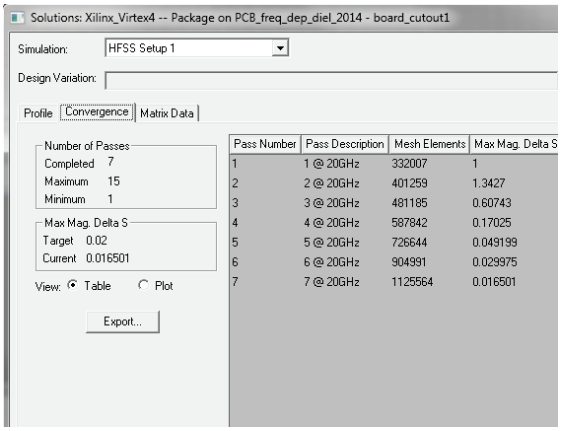

Figure 7. Convergence table

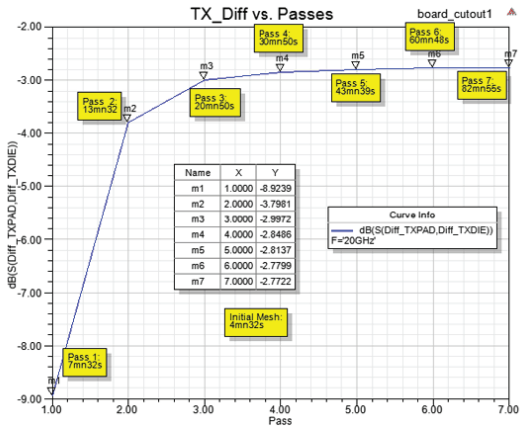

Figure 8. Insertion losses of TX differential pair vs. passes

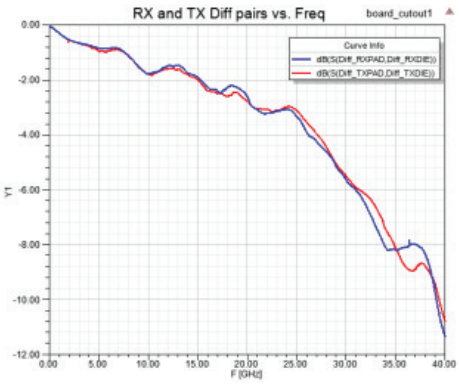

Figure 9. Insertion loss of two differential pairs vs. frequency

Simulation

The first part of this paper highlighted how important it is to provide automation and a user-friendly interface to board and package designers. The traditional heavy weight classic 3-D electromagnetic simulator user interface is one of the main impediments preventing more wide spread use of these tools by the non-expert users. Another barrier is illustrated by this question: "How long will it take to run my simulation and analyze my results?" ANSYS HFSS 3-D layout answers this question with "Much faster than you would expect," thanks to the following items:

- Automatic adaptive mesh that warranties the optimum mesh for the requested accuracy
- Phi mesher specifically dedicated to layered structure
- High-performance computing that allows multi-threading and solving frequency points in parallel on different cores and computers

The automatic adaptive mesh process is based on iterative mesh refinement, which identifies the region where the mesh needs to be refined to reduce the error between two solutions. Figure 7 shows the convergence table that illustrates progression of the adaptive mesh process. Convergence is achieved after seven passes, reaching an error close to 0.01 with a number of mesh elements slightly over 1 million. Figure 8 shows the insertion loss of a TX differential pair connecting package and board, at 20 GHz (adaptive frequency) versus adaptive passes. The adaptive process was performed using 16 cores. Using the Phi mesher, the initial mesh was created in less than five minutes; in the past, it took significantly longer with the standard classic mesher. The third pass is achieved after 21minutes with a value of +/-10 percent to the final solution, which means that in 20 minutes you can complete a sanity check on this complex design. The fifth pass is achieved after 44minutes with a value less than +/-2 percent to the final solution. Value variation between passes five, six and seven shows that convergence is achieved, ensuring the optimum mesh for selected accuracy in 1 hour 20 minutes.

Initial Mesh Generation

For layered geometries such as PCBs, packages and ICs, the phi mesher provides extremely fast generation of an initial conformal tetrahedral mesh. These structures can often exhibit a high degree of geometric complexity associated with the numerous traces, vias, pads and solder balls or bumps. This complexity can result in initial mesh generation times approaching or even exceeding the total time for the electromagnetic simulation itself. Unlike traditional finite element meshing technologies that make no assumptions about a given geometry, the phi mesher takes advantage of knowledge regarding the stacked-up nature of these layered designs. The phi mesher decomposes the layers into a set of convex polygons from which 3-D convex polyhedrons are derived to fill the volume within the layers, which are then further processed into conformal tetrahedrons for the initial 3-D tetrahedral mesh. This algorithm avoids the expensive and time-consuming creation

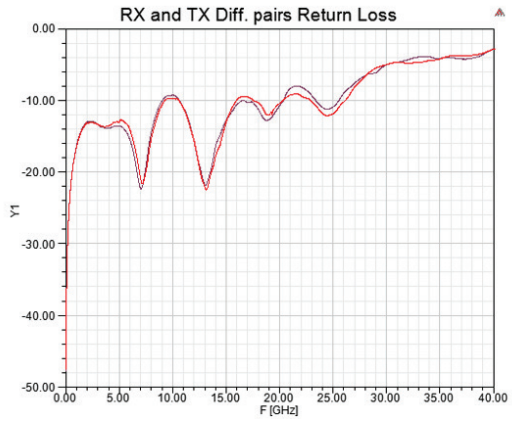

Figure 10. Return loss of two differential pairs vs. frequency

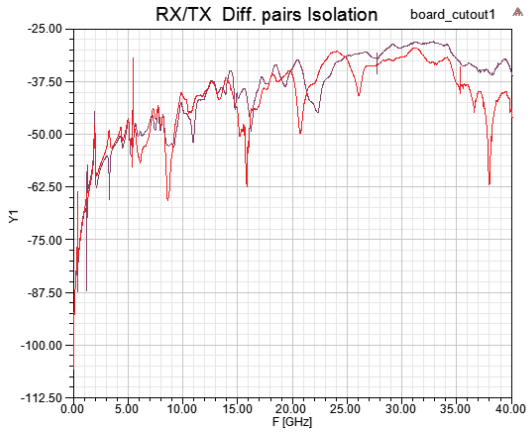

Figure 11. Insertion losses of TX differential pair vs. passes

and destruction swapping processes common in 3-D FEM meshing. All complex calculations are performed in 2-D instead of 3-D, providing further robustness and scalability to the algorithm. The end result is that for these types of complex layered structures, the phi mesher can reduce mesh times by a factor of 30 or more when compared to general-purpose 3-D FEM meshing techniques.

Simulation Results

A frequency sweep from 0 GHz to 40 GHz was run to extract the s-parameter model in the requested bandwidth. Post-processing allows automatic identification of differential pairs from single-ended terminal. Results can be plotted as single-ended terminal or differential pairs. Various results are shown (Figure 8 insertion loss in dB; Figure 9 return loss in dB of the two differential pairs, receiver (RX) and transmitter (TX); Figure 11 isolation between RX and TX differential pairs). Depending on the specification, the designer will identify the frequency range of usage for the package on board device.

Summary

ANSYS HFSS 3-D layout offers an innovative process for package, IC on printed circuit board simulation and extraction. The powerful automation allows designers to quickly and easily transfer the board and package design from their existing layout design flow to the 3-D electromagnetic simulator, ready for simulation. Automatic adaptive meshing processes, faster meshing and high-performance computing capabilities provide the accuracy level and speed required into today's compressed and competitive design cycles.

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