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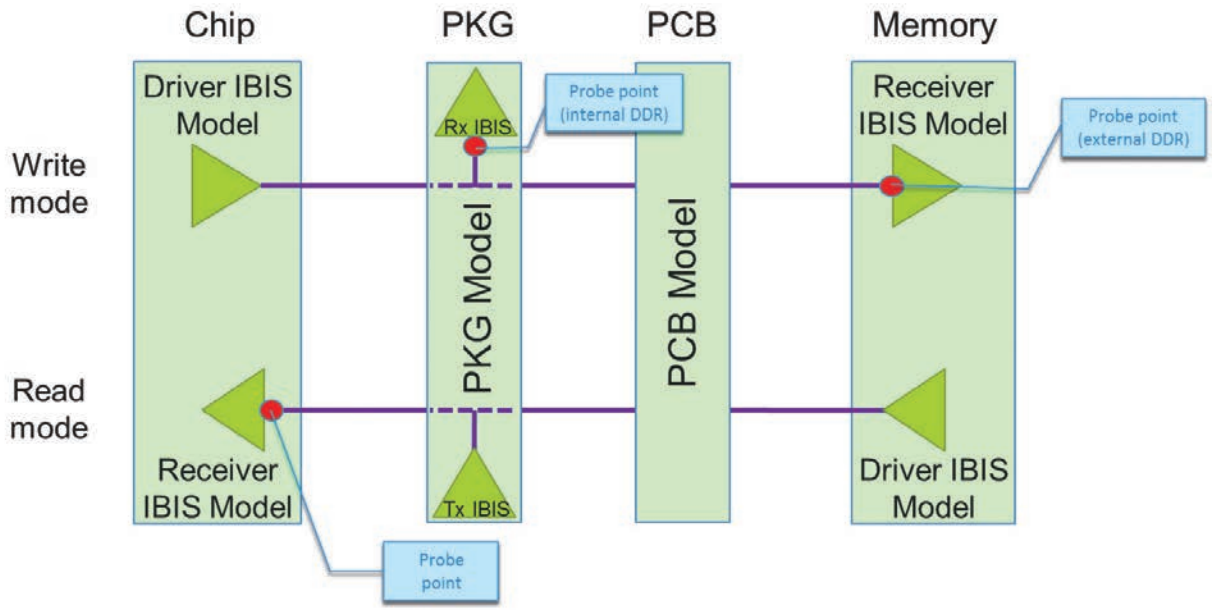
MAINTAINING POWER AND SIGNAL INTEGRITY

The ever-changing hardware that supports big data and the Internet of Things must be fast, reliable and quickly developed.

By Larry Zu, President, Sarcina Technology LLC, Palo Alto, U.S.A.



▲ Bidirectional channel simulation environment for SiP package

Every few years, a new electronic invention changes our lives. These devices and services rely on powerful data centers, which demand robust chips as well as high-speed interconnects and input/output (I/O). Accordingly, the printed circuit boards (PCBs) must be powerful and well-designed to provide quality solutions for power integrity and signal integrity. Additionally, all connectors and electrical and optical cables connected to the PCB must provide a reliable environment for high-speed digital signals.

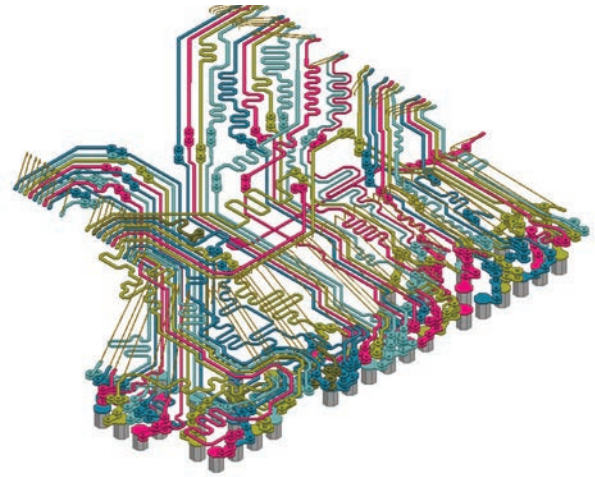
To keep pace with big data and the Internet of Things, PCB/chip speed and reliability are paramount. To meet aggressive specifications, engineering teams need accurate simulations to validate and improve designs before they are taped out — and well before prototyping.

Sarcina Technology has expertise in designing high-performance, application-specific integrated circuits (ASICs) and their PCBs. The company employs state-of-the-art simulation tools from ANSYS for these challenging tasks.

TO SIMULATE OR NOT

Simulation software gives engineers the ability to do amazing things. However, having that capability may require a significant outlay of funds for both software and necessary engineer training. This raises the question: Is simulation software worth the increased non-recurring engineering cost?

Electrical simulation software gives designers all the tools needed to successfully design complex products the first time, every time. For instance, electronics developers at Sarcina Technology use the ANSYS HFSS 3-D full-wave solver for modeling because of its accuracy and reliability. An organization can use a variety of factors — including competition, price, profit margin, design constraints and system intricacies — to determine if simulation software is the right choice.



▲ 3-D view of LPDDR package model

To keep pace with big data and the Internet of Things, PCB/chip speed and reliability are paramount.

ANSYS HFSS 3-D LAYOUT
ansys.com/83power

BIDIRECTIONAL CHANNEL FOR SYSTEM-IN-A-PACKAGE (SiP)

The ASIC chip inside an SiP can communicate with either the internal low-power double data rate (LPDDR) die inside the

SiP or an external LPDDR memory chip on the PCB. Since there is no termination for the first generation of DDR, large ripples are anticipated at the LPDDR receiver side, both inside and outside the SiP package. In addition, the LPDDR operates at the smaller 1.8 volts, as opposed to the traditional 2.5 volts. This further reduces the voltage swing and makes the receiver eye diagram appear even worse. Because of these factors, Sarcina Technology ran rigorous bidirectional channel simulation for the design of an SiP package with its PCB.

The engineering team imported a 3-D model of the LPDDR package from Cadence® Allegro® Package Designer software using the ANSYS ALinks for EDA translator and editor. The model was then ported to ANSYS HFSS to provide a full-wave S-parameter model for simultaneous noise switching analysis. The team then simulated this S-parameter model with read-and-write mode for data, strobe, address, command, control and clock signals for both internal and external LPDDRs.

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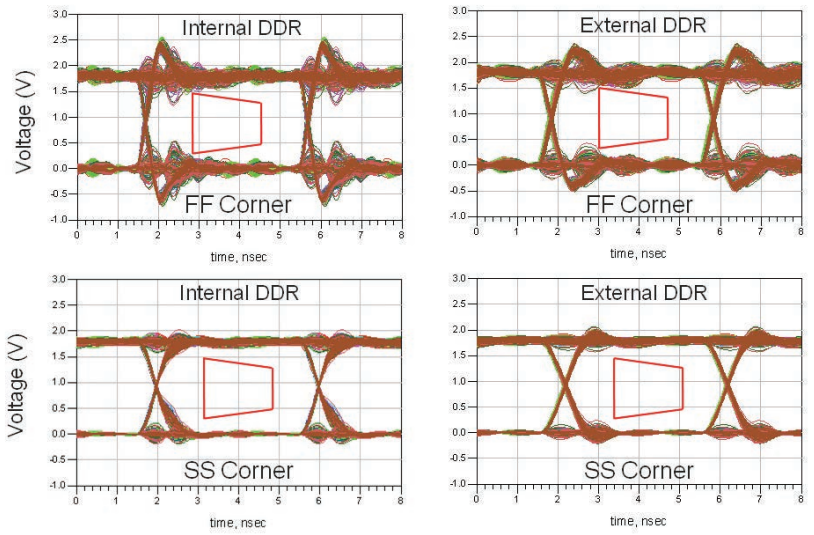
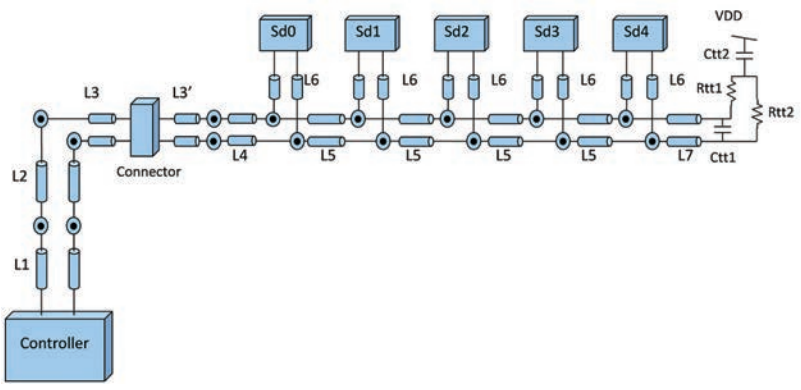


▲ Simulated eye diagrams for internal and external LPDDRs under FF and SS corners. The FF corner has more ripples than the SS corner due to faster edge rate.



▲ DDR3 differential clock net's topology for designed PCB and its daughter card from ASIC chip's controller to termination at daughter card. During the daughter-card layout, Ctt1 was inadvertently placed on the board, which shifted the clock and clock# crossover point in the eye diagram and violated hold time.

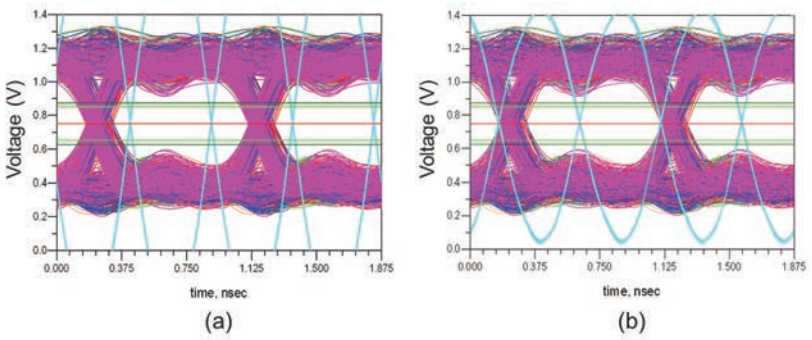
Eye diagrams at both the internal LPDDR die and external LPDDR chip were captured. The Sarcina team observed that, contrary to conventional thinking, the silicon wafer FF (fast P-type and fast N-type transistors) process corner had the worst eye diagram. This is because the fast edge rate at FF wafer corner introduces higher ripples. As a result, the eye diagrams are dramatically worse than the SS (slow P-type and slow N-type transistors) corner. In actuality, the SS corner has the best eye diagrams, even better than those of the TT (typical P- and N-type transistors) corner. This is due to the slower rising and falling edge rates, which help reduce ripples when no termination is present for LPDDR architecture. Through this simulation, Sarcina Technology's engineering team learned that it must use higher-grade LPDDR die, which requires smaller setup and hold time and, as an added benefit, gives more margin to the simulated eye diagram. Subsequent automatic test equipment debugging results showed that the higher-grade LPDDR was necessary for the SiP to pass DDR read-and-write tests. This simulation gave Sarcina Technology the rationale to order the higher-grade LPDDR wafer, which it would not have done without rigorous DDR channel simulation. The simulation helped the engineering team come up with a successful system on the first try.

DEBUGGING A PCB DESIGN

Sarcina Technology's engineers also use electrical simulation in debugging PCB designs before the boards are assembled. This helps to avoid post-assembly lab debugging, which can be quite expensive and time-consuming. Data center customers demand first-time success in chip, package and PCB designs to meet the increasing demands of big data for large data transfers.

For example, consider the design of a DDR3 differential clock network topology for a potential PCB that includes a daughter card containing several DDR3 memory chips. The ASIC DDR3 controller (inside the ASIC chip) is on the main PCB board. During the daughter-card layout, a decoupling capacitor was inadvertently placed on the board. During post-layout DDR3 channel simulation for the address bus, the engineering team realized that the clock and clock# crossover point could not be positioned at the center of the address eye diagram because this created a hold-time violation.

After reviewing all simulation schematics and layouts in the PCB and its daughter card, the misplaced capacitor was revealed. Engineers used ANSYS SIwave to extract DDR3 electrical models for both PCB and daughter card. The extracted models allowed the team to perform what-if analyses with and without the capacitor to quickly identify the cause of the problem. Following removal of this capacitor from the simulation, the clock and clock# crossover point was repositioned close to the center of the eye diagram, which met both setup and hold-time specs.



▲ DDR3 address simulated eye diagram with (b) and without (a) removal of capacitor Ctt1

Whether designing an LPDDR layout with ANSYS HFSS for simultaneous switching noise analysis or extracting DDR3 electrical models with ANSYS SIwave, Sarcina Technologies utilizes ANSYS simulation solutions to meet the ever-increasing demands of customers that develop the chips, packages and PCBs required by big data and the Internet of Things. Simulation is important to ensure first-pass success.