Multiphysics Simulations for RFICs and SoCs for 5G Applications

System-on-chips (SoCs) and radio frequency integrated circuits (RFICs) for 5G smartphones and networks need to manage huge amounts of antenna data and offer significantly high processing capabilities in thermally and power-constrained environments. ANSYS multiphysics simulations simultaneously solve power, thermal, variability, timing, electromagnetics and reliability challenges across the spectrum of chip, package and system to promote first-time silicon and system success.

Semiconductors
The complexity of 5G is reflected in the SoCs that will power 5G smartphones/user equipment (UE) and radio access network (RAN)/network infrastructure elements. 5G base station and mobile chipsets should support smart beamforming and beam tracking/steering capabilities to increase millimeter-wave (mmWave) coverage and minimize interference. Complex 3D antenna arrays with automatic beamforming used in the implementation of massive multiple-input and multiple-output (MIMO) antenna consume significant power (80-plus W). Combined with other sensitive analog and radio frequency (RF) circuitry, these elements make up the RF front-end components, providing a fully integrated mmWave RF solution.

There are three beamforming architectures: analog, digital and hybrid. In terms of power, complexity and capacity, each of these architectures has pros and cons. For example, digital beamforming architectures offer the highest capacity and flexibility but consume more power compared to analog and hybrid architectures.

Moreover, 5G baseband chips, beamforming modules and SoCs require process nodes that are leading-edge, performance-based (FinFET 14nm – 7nm and lower, power-efficient silicon-on-insulator (SOI)-based) and have advanced packaging. For these designs, the margins are smaller, schedules tighter and costs higher. The growing interdependence of various multiphysics effects like timing, power, electromagnetics, thermal and reliability in sub-16nm designs pose significant challenges for design closure. Traditional margin-driven, silo-based design approaches to the chip, package and board lead to suboptimal designs. These solutions have limited simulation coverage that fail to unravel potential design weaknesses, causing field failures.

This white paper delves into early power efficiency, power integrity, reliability, advanced packaging and electromagnetic crosstalk analysis requirements for SoC and intellectual property (IP) designs.

Early Power Analysis
A shift from 4G to 5G is expected to deliver a hike in cell edge data rates from 10 Mbits/sec to more than 1 Gbit/s, plus a 50% gain in energy efficiency. With each generation —3G, 3.5G, 4G and, now, 5G — the peak-to-average power ratio (PAPR) has been continually increasing.

For evolving generations of 5G implementations, the main focus is on predicting power profiling early in the chip design phases, especially in the following key areas:

- Spectrum-related issues
- Traffic characteristics
- Radio interference and interoperability
- Network access-related issues

Power efficiency is a key design consideration for 5G devices. Average power, peak power, peak change in power and sustained worst-case average power are all important for thermal robustness, power integrity and cost of operation of 5G systems. Early feedback is critical to achieving 5G power targets. ANSYS PowerArtist helps designers address power early in the register-transfer level (RTL) design phase to create power-efficient products for 5G applications.
5G SoC Solutions

- PowerArtist provides 7/5nm-proven RTL power accuracy within 15% of gate-level power by modeling the physical effects of clock tree, wire capacitance and multibit flops. Turnaround time is 20-times faster than traditional gate-level methods. This enables designers to identify and make power decisions early and reliably. By uncovering power reduction opportunities, such as hierarchical clock gating through RTL techniques and powerful interactive debug and power-efficiency metrics, PowerArtist enables power savings as high as 70%.

- PowerArtist also accelerates power profiling that runs several orders of magnitude faster than traditional interval-based power analysis methodologies. This rapid analysis cuts analysis time from weeks to hours — to facilitate the identification of critical peak power and large current transient (di/dt) cycles that can cause excessive voltage drops and, potentially, timing failures. Critical cycle selection is important not only for focusing power reduction efforts, but also for guarding the chip against design failures due to undetected scenarios for robust power and thermal planning across the chip, package and system.

Consider an example where mobile phone users — in a fast-moving train, using Gbps data rates — encounter a change in base station. This will lead to large step functions in power as the new base station establishes the connections and starts to serve this large set of users, while the previous base station releases the connections. The 5G systems must naturally be able to serve such needs with sub-1 ms low latency. With fast power profiling and efficient activity transfer flows with emulators, PowerArtist can generate per-cycle power profiles for millions and billions of cycles of activity. This makes analysis possible early at RTL, when meaningful high-impact design changes can still be made.

Power Integrity Issues in 5G SoCs

For 5G SoCs, power grid signoff through traditional approaches is not feasible. This is due to severe routing constraints that can potentially cause timing convergence issues downstream. For advanced FinFET technology processes, the power grid's node count is very high and any reduction in node count will affect accuracy. With very small design margins, power signoff solutions leave little margin for error. The slightest inaccuracy can result in product failure. It is important, therefore, to analyze the entire power grid flat rather than partitioning the design with a “divide and conquer” approach.

Scalability across thousands of cores using ANSYS SeaScape big data technology helps signoff a billion-plus instance design in a few hours on commodity hardware. Different simulation modes — RTL and gate vectors, smart vectorless analysis for functional and scan mode, mix-mode simulation (vector-less plus value change dump (VCD)) and power-transient and power-up analysis allow increased design coverage for power integrity signoffs.

Moreover, ANSYS semiconductor solutions provide data analytics, which offer valuable insights into design weaknesses. Customizable analytics help create unique metrics to represent design quality based on physical, electrical and other simulation parameters. For instance, fixing low timing slack paths going through a high dynamic voltage drop area requires knowledge of all timing paths and all voltage drop scenarios. A targeted design-fixing approach with these analytics is more efficient at prioritizing and fixing issues at 7nm.
Addressing SoC Reliability Issues

Design for reliability is a key consideration for advanced SoCs used in 5G communication systems. These SoCs, for example, will be instrumental in enabling mission-critical applications of the future like self-driving cars. Reliability issues can be challenging at advanced FinFET nodes. FinFET designs have high dynamic power density, and power directly impacts the thermal signature of the chip. Accurately modeling the temperature distribution on-chip by considering the chip in the context of the system is critical for ensuring its reliable operation. Higher temperature, higher current and thinner interconnects are pushing the limits for electromigration (EM) failures on-chip. Thermal issues are very serious because in advanced FinFET technology nodes, self-heating and joule heating can cause local temperatures to rise greater than 10°C. This happens because the surrounding materials of low K dielectric cannot dissipate the heat well into the silicon substrate, so heat gets trapped in the wires and devices. This high delta-T may lead to EM failure on the chip interconnects/device layers. Extra efforts are required to quantify the temperature rises on devices and wires. ANSYS RedHawk and ANSYS Totem provide full support for thermal-aware power/ground and signal line EM verification. These solutions accurately analyze EM violations while minimizing false positives for advanced FinFET-based designs.

A thermal-aware EM solution for modeling self-heat effects and overall junction temperature variation of the die is required for an accurate signoff methodology. In addition, statistical electromigration budgeting (SEB) allows chip designers to meet the stringent safety and reliability requirements, by prioritizing the most important EM fixes for signoff while avoiding overdesign. Designers can benefit greatly from SEB modeling by fixing only the most critical EM violations that impact product reliability. This significantly helps in cutting months of reliability signoff effort down to a few weeks and accelerating design closure.

RedHawk and Totem self-heat and chip-package thermal co-analysis solutions are supported for advanced FinFET technology nodes (N16 and below) across all major foundries.

With the prominent use of IPs and high-speed interfaces in SoCs, electrostatic discharge (ESD) design and verification is becoming extremely challenging. ESD checks are now one of the key signoff metrics. Almost 55% of the failures are interconnect-related, and can be avoided by performing systematic ESD checks during the design phase. But ESD protection that works at the IP level may not work at the SoC level due to poor connectivity to other IPs and circuits in the SoC. Therefore, it is important to analyze the ESD protection schemes at the SoC level, across multiple voltage domains, to make sure they provide the intended low-resistance path for discharging a potential ESD event without stressing the functional devices.

ANSYS PathFinder enables fully distributed machine processing to achieve full-chip, flat ESD signoff for billion-plus instance designs. PathFinder Explorer — the GUI-based interactive debug feature — promotes rapid design exploration and data mining to gain key insights into design issues for prioritizing design fixes. Dynamic ESD analysis now supports FinFET designs. Pathfinder can generate chip ESD compact models (CECMs) for system-level ESD/electromagnetic compatibility (EMC) simulations.

Device aging is another area of concern for reliability, as baseband chips placed in telecom towers need to operate reliably for many years. Aging refers to device degradation with time. Electric fields across transistor gates slowly degrade the dielectric of the device. Main physical effects are bias temperature instability (BTI) and hot carrier injection (HCl). Electrically, this manifests itself as a shift in threshold voltage, resulting in reduced drive currents over time. This, in turn, causes more delays, eventually causing timing failures. Aging effects typically occur over several years after the chip is in production; typically, these show up as slow degradation of individual transistor performance. Some transistors may significantly degrade while similar transistors might not be impacted. The aging phenomenon is extremely sensitive to usage patterns. Common design techniques, such as clock gating, can exacerbate the problem. ANSYS Path FX provides device aging simulation capabilities for leading-edge designs.
Advanced Packaging Challenges

Advanced packaging technologies will be the key driver of heterogeneous integrations in next-generation edge compute data centers and 5G electronics systems to achieve extreme performance, high system bandwidth, low power and low cost. The internet of everything – enabled by 5G infrastructure – will generate huge amounts of data to be processed and stored. The ability to handle such large volumes of data will be threatened by limited system bandwidth between the traditionally packaged processor and the memory that is integrated into the system. Hence, advanced 2.5DIC/3DIC packaging technology — including through silicon vias (TSVs), die and wafer stacking, system-in-package (SiP), package-on-package (PoP), advanced wafer-level packages (WLP) and interposer integration that leverages the third dimension for scaling — will become a popular choice for 5G system designs. Short interconnection paths enabled by TSVs between stacked chips lead to higher performance because of increased I/O speed. They also consume lower power due to reduced capacitance and smaller form factor due to stacking multiple dies. This is indeed a very promising technology, although it is fraught with many challenges due to its complexity. ANSYS offers comprehensive chip-package-system (CPS) workflows for solving thermal, power and signal integrity issues for chip-aware systems and system-aware chip signoff.

Substrate Noise Analysis for mmWave RF Solutions

Integrating a high-power beamforming module with sensitive analog and RF circuitry can lead to substrate noise propagation from the beamforming module to analog/RF circuitry and vice versa, which can impact the overall performance. For accurate power noise analysis, it is important for a designer to model the propagation of substrate noise in DvD analysis. Integrating the digital beamforming module with sensitive analog and RF circuitry that makes up the RF front-end module can cause switching noise to propagate through the substrate if enough isolation is not guaranteed.

For reliable operation of the mmWave RF module, it is critical to have a methodology that allows for modeling of the substrate noise generated in a digital beamforming module using digital noise injection. The methodology must also perform analysis to determine the frequency and time-domain response of the analog/RF blocks. It is important to adopt the right isolation techniques for a specific technology node by planning the isolation structures such as p-guard ring, deep n-well tub, deep n-well guard ring, etc., early in the design cycle using test structures to avoid any surprises later during signoff.

Substrate noise analysis requires a true mixed-signal power noise and reliability analysis solution. ANSYS Totem is the industry’s only mixed-signal EM/IR tool with a track record of foundry signoff for substrate noise analysis. It helps assess the noise impact on timing, frequency domain analysis and the quality of the guard ring, leading to faster signoff closure.

Electromagnetic (EM) Analysis in RFIC and SoC Designs

For 5G, radio frequency front-end circuits, high-performance reference oscillators and associated interconnects must be designed properly to ensure reliable operation at 6 GHz and up to mm-wave frequencies. On-chip mixed signal components are affected by electromagnetic effects and their design considerations should include self- and cross-coupling among various sensitive mixed signal circuit blocks. Careful examination of the layout, parasitic inductance and capacitance, substrate modeling and trace resistance is critical for reliability.
The need to model electromagnetic effects from DC up to mm-wave frequencies calls for special handling of layouts. ANSYS has several advanced EM simulation technologies that can be leveraged for on-chip structures. ANSYS HFSS is the gold standard finite element method (FEM) extractor that experienced engineers rely on for technology exploration and signoff validation. With new tools added from ANSYS’ acquisition of Helic, Inc., engineers can create scalable models of on-chip components like capacitors and inductors. In these tools, a novel, full-3D meshing algorithm segments the conductors’ volume into small cells suitable for accurate modeling of capacitance, inductance and resistance. The engine computes all the layout dependent effects (LDE) before the meshing step. In addition to LDE, users can accurately model and characterize power/ground nets, bond/bump pads, decoupling capacitors, seal rings, metal fill, package layers and spiral inductors.

The 3D capacitance extraction methodology uses a sophisticated stochastic sampling algorithm based on the random walk theory, for calculating the electric field along the Gaussian surfaces and corresponding coupling capacitances between arbitrary shaped conductors. Distributed 3D electric fields are captured with great accuracy using stochastic sampling and the sophisticated numerical solution of multilayer Green's function. The method does not use any kind of pattern matching look-up tables or averaging, and it is free of conductor discretization bottlenecks. These solutions provide optimum computing efficiency since random walk is an inherently parallel and extremely fast algorithm.

This unique extraction engine models substrate coupling effects with a distributed RC network. A stochastic Monte Carlo-based methodology and a 3D substrate model allows for fast and accurate extraction of the distributed RC substrate network. The method employs a random walk algorithm to characterize multiple substrate layers using appropriate Green's functions without the need of 3D discretization. The parallel nature of both capacitance and substrate modeling algorithms offers superior scalability and reduced extraction times.

For inductance and resistance modeling, ANSYS on-chip electromagnetic (EM) solutions combine the accuracy of a full-wave EM modeling engine with the flexibility of SPICE netlist output. Extracted models fully capture inductance and resistance behavior from DC up to mm-wave frequencies. These solutions capture all electromagnetic phenomena — including current distributions, skin and proximity effects — and are extremely accurate for mitigating the risks of electromagnetic crosstalk, induced performance degradation and failure in high-speed and low-power system-on-chip designs.

Conclusion
The transition to 5G is exciting, but it is no small task given the degree of complexity at various points in the system. The ANSYS 5G solution provides a compelling set of design solutions from SoCs to mobile UE to networks and beyond. ANSYS multiphysics solutions are built on this set of trusted ANSYS products and capabilities:

- **ANSYS RedHawk-SC** — for reliable low-power design and power integrity of SoCs
- **ANSYS Totem** — for transistor-level power noise and reliability simulation of IP blocks, analog, mixed-signal and custom digital designs
- **ANSYS PowerArtist** — for early RTL power analysis and reduction
- **ANSYS VeloceRF, ANSYS RaptorX, ANSYS Exalto** and **ANSYS Pharos** — for designing and selecting on-chip mixed signal components and evaluating electromagnetic crosstalk effects among sensitive mixed-signal circuit blocks
- **ANSYS Icepak** — for thermal integrity applications on antenna systems and data processing hardware
- **ANSYS Mechanical** — coupled with ANSYS Icepak, for structural reliability of 5G systems

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