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KEEP THE NOISE DOWN

ANSYS electronics tools work together to solve coupled power integrity and signal integrity problems in designing robust electronic systems.

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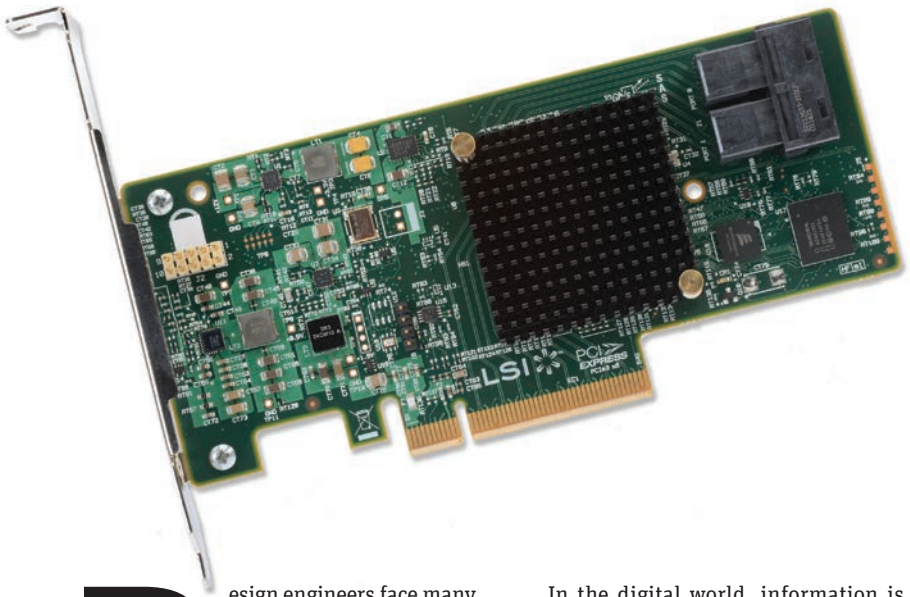


LSI DISCUSSES ROBUST ELECTRICAL AND ELECTRONICS SYSTEM DESIGN
ansys.com/82noise

Design engineers face many challenges as they create robust electronic systems. In this era of low-power design and high-speed circuits, poor power and signal quality can result in design failures that lead to performance degradation and malfunctioning devices. Maintaining signal integrity and power integrity across the entire design, from chip and package to system, ensures delivery of robust electronic products.

In the digital world, information is transmitted in a sequence of 1s and 0s. In an ideal electronic transmission, the 1s are conveyed by trapezoidal waveforms that rise from 0 to a specified voltage, and the 0s get conveyed by signals that fall from that voltage to 0 (bit 0) in a specified time. In the real world, there is nearly always some deviation from this ideal signal. The deviation of signal amplitude from ideal voltage is simply called noise, while the deviation in time is jitter. In the presence of jitter and noise, the signal's rising and falling edges can move along the time axis, and the voltage level can move along the amplitude axis, to such a degree that the required bit detection conditions will not be satisfied. This results in data transmission corruption and eventual system failure. Both noise and jitter in the signal can arise for multiple reasons — however, the primary causes tend to be fluctuations in the power supply no matter how carefully designed (power integrity) and the coupling that happens between the various power and signal interconnects present in electronic systems (signal integrity).

To manage such complexities, LSI Corporation uses ANSYS tools to model the behavior of a system on a chip (SOC) under load; engineers also diagnose and solve both power integrity and signal integrity issues in a single environment. LSI designs semiconductors and software that accelerate storage and networking in datacenters, mobile networks and client computing. The company developed a methodology to address power and signal integrity issues in a holistic manner by leveraging ANSYS chip–package–system

ANSYS simulation technologies were used to guide the redesign of the chip–package routing to eliminate noise and PLL failure.

This methodology highlights the importance of simulating systems-level interactions.

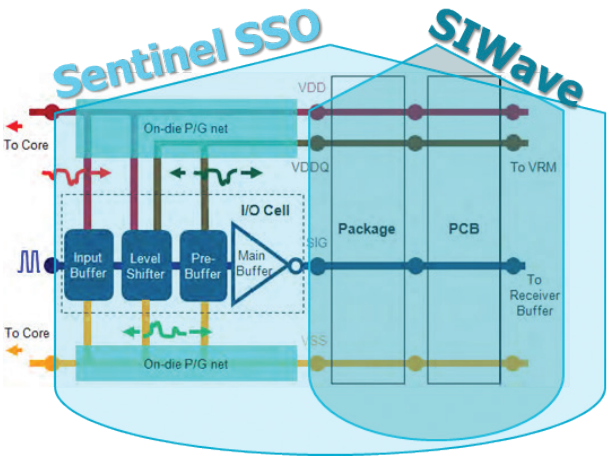
solutions. In this workflow, ANSYS Sentinel-SSO (for chip-level timing and noise analysis) is coupled with ANSYS SIwave (for printed circuit board–level noise analysis) to help predict noise generated by the switching activity of independently supplied I/O cells and its effects on the dedicated supply for phase-locked loops (PLLs). In application, the analysis showed that voltage swings on the signal network of a DDR parallel interface circuit were coupling to the power supply of the PLL, resulting in phase error between the PLL reference clock and output clock. Silicon measurements confirmed that the PLL unlocks were associated with DDR output buffer-induced noise. The LSI team subsequently used ANSYS simulation technologies to guide the chip–package routing redesign to eliminate this coupling and PLL failure.

ADOPTING A NEW VERIFICATION METHODOLOGY

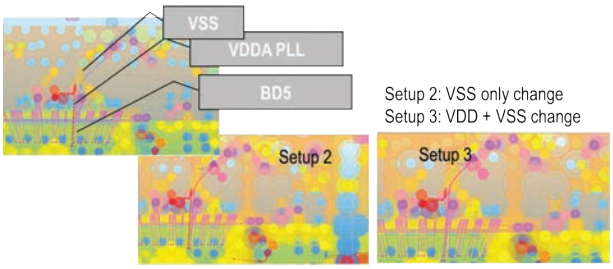
LSI's traditional design verification methodology involved assembling a system representation from package and PCB models. This traditional approach addressed AC ripple voltage caused by digital switching activity but did not take into account custom I/O switching activity or analog clocks. Package-to-PCB discontinuities are not captured with the traditional method, since the PCB and package models are extracted separately. As a result, the process underestimates the effect of discontinuity between package and PCB.

Engineers at LSI developed a more comprehensive design verification methodology that utilizes ANSYS Sentinel-SSO and ANSYS SIwave to evaluate the effects of DDR I/O switching activity on PLL supply noise. Sentinel-SSO is a high-capacity I/O subsystem timing and noise analysis solution for IC and package–system integrity designers. SIwave is a specialized platform for signal integrity and power integrity analysis of electronic packages and PCBs. Engineers generated nonlinear package load-independent models of the I/O buffers (chip I/O model) in Sentinel-SSO. Separately, they extracted the on-chip I/O ring PDN parasitic and optimized using model-order reduction techniques for inclusion with these I/O buffer models. In parallel, engineers extracted the package and PCB models using SIwave. I/O buffer models and the I/O ring PDN parasitic model were then combined and integrated with the package and PCB models inside Sentinel-SSO to perform a simultaneous chip–package–system power- and signal-integrity analysis. By using I/O chip I/O models, an entire bank of I/O buffers can be simulated unrestricted by SPICE simulation capacity or run-time limitations. Simulating the entire bank in one simulation environment provided benefits beyond predicting noise in the power/ground networks: LSI engineers were able to assess the impact on signal propagation as well as perform design fixing and exploration for both chip and package–PCB design.

The engineering team set up the project using the Sentinel-SSO graphical user interface. The software allowed for rapid inclusion or exclusion of I/O that were not critical to the analysis and provided an in-depth dive into the layout. The team viewed the physical chip layout and easily checked for problems, such as missing vias and poorly connected decoupling capacitors, before the simulation was run. They used the schematic to probe nodes and add stimulus and models to the system setup. Sentinel-SSO allows for simulation with native transistor models of I/O buffers, providing a one-time qualification of chip I/O models.



▲ Sentinel-SSO model of die coupled to SIwave model of package and PCB



▲ LSI evaluated three different package routing iterations.

EVALUATING THREE PACKAGE DESIGNS

The engineering team created three different package models in SIwave; each included full and compact models of a package mounted on a PCB model. These models accounted for all data bit, address bit and control bit lines as well as PDN and PLL supply coupling and the characteristics of the system-level ground. Engineers extracted the S-parameter touchstone format model from each model and plugged it into Sentinel-SSO.

Package 1 was based on the original package in which the PLL positive supply voltage (VDDPLL) was a separate supply, with two

Chip–package–system cosimulation made it possible to pick the best choice from three different package options.

wire bonds augmented by negative supply voltage (VSS) wire bonds on the left and the bit line (BD5) on the right. VDDPLL was adjacent to the analog positive supply voltage (VDDA1.8) at the via and power-plane level in the package. In package 2, the adjacent VSS wirebond was removed to test the theory that ground noise was inducing the PLL unlocks. In all other respects, package 2 was identical to package 1. Package 3 also had the adjacent VSS wirebond removed; in addition, VDDPLL was shorted to VDDA1.8 to explore the possibility of reducing VDDPLL noise by lowering its impedance.

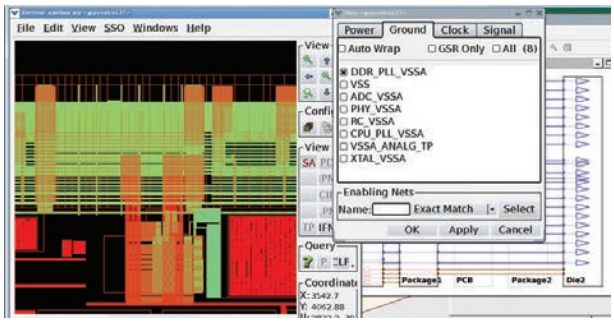
Because the original extraction of the full on-chip PG network created a network with many nodes, engineers synthesized a reduced-order model. This model was orders of magnitude smaller and more efficient to simulate. Using the state-space method, the team constructed a chip I/O model from neural networks. The approach greatly accelerated the analysis workflow without compromising simulation fidelity. For example, a 100 ns simulation run using the I/O buffer transistor models traditionally took 64 hours. In contrast, the same simulation run took only 24 minutes using chip I/O models. This magnitude of improvement is typical.

Simulation results showed that the current return path was different for DC and low-frequency versus high-frequency signals. The mutual coupling among VDDAPLL, BD5 and VSS wirebonds was dominant at high frequencies. The capacitive coupling between VDDAPLL and VDDA1.8 was dominant at clock frequency.

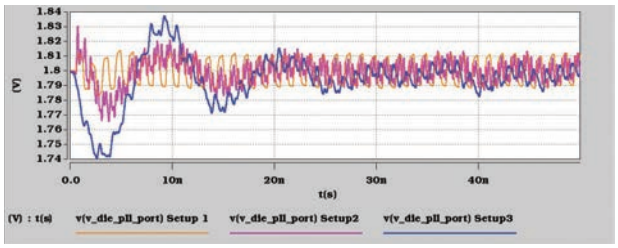
Time-domain simulations showed that package 2 provides the cleanest VDDPLL supply. A frequency-domain simulation indicated that a noise reduction of about 10 dB could be expected on the PLL supply with package 2, and this would be enough to eliminate the PLL unlock events. This improvement is achieved only at the main clock frequency of 800 MHz. At higher frequencies, the current return paths are different, and the package 2 solution enables mutual noise coupling through other avenues.

CORRELATION WITH PHYSICAL EXPERIMENTS

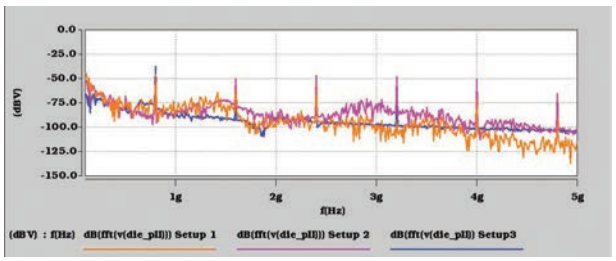
The team tested packages 1 and 2 in the lab using a series of DDR read/write transactions. The tests correlated well with simulation, showing that noise on DDR_PLL_VDA and DDR_PLL_VSSA caused phase error between the PLL reference clock and output clock. When phase error between the PLL reference clock and the output clock reached a limit of +/– 6 times the reference clock period, loss of clock detect for the dedicated I/O of the output interface of the CCG block was asserted indicating a phase mismatch that exceeds the limit. The time interval error showed long-term clock drift. Both the lab result and simulation agreed that PLL_VSSA suffered from ground bounce because of simultaneous switching noise (SSN) and a high concentration of return current from DDR data signals. In package 2 with PLL_VSSA shorted to chip VSS, the PLL_VSSA bond wire was much shorter, reducing impedance and ground bounce.



▲ The PLL supply separated from the 1.8 V analog supply was included in the layout extraction.



▲ Time domain comparison for VDDPLL noise



▲ Frequency domain comparison of VDDAPLL noise

Chip–package–system cosimulation methodology used by LSI engineers showed how power- and system-integrity analyses can be combined to evaluate the supply noise effects seen by a PLL device at the metal 1 layer level. It also demonstrated how noise on the PDN was analyzed and quantified — noise that could not be found with any other tool or methodology. This technique highlights the importance of simulating system-level interactions. Although the switching data bit lines are only infinitesimally coupled to the dedicated VDDPLL on die, they are strongly coupled to the VDDPLL on the package and in the PCB. By using this methodology, it was possible to pick the best choice from three different package options. Using coupled power- and signal-integrity simulation saved LCI one design iteration cycle, or a week of work.