Ensuring Chip Level ESD Integrity

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What is ESD?

**Electrostatic Discharge**

“A transfer of charge between two bodies at different electrostatic potentials, either through contact or via an ionized ambient discharge (a spark).”

High current event causing latent or catastrophic failures to IC

Drain/Source junction or gate-oxide damage

Metal/via melt-down

Intended path

Unintended path
What is ESD?

**Human Body/Machine Model (HBM/MM)**

**Charged Device Model (CDM)**

Discharge currents for different types of ESD events

PathFinder™: SoC and IP ESD Integrity

- Layout (DEF/GDS)
- Technology
- Spice Netlist/Clamp Models
- ESD rules

**Layout Connectivity Checks**
- Resistance Checks
- Interconnect Failure Checks
- Dynamic Checks

**Dynamic Checks**
- Monitor device stress

**Root-cause Analysis**
- IP/Full-chip Capacity
- Early Stage to Sign-off

- PathFinder

- **Electromigration Map**
- **Macro Block**
- **Substrate RC**
- **Well Diode**

- **Zap**
- **RC**
- **VDD**
- **GND**

- **Any Point**

- **Interconnect Failure Checks**
- **Resistance Checks**
- **Layout Connectivity Checks**
Common ESD Issues in SoCs

ESD Failure Types

- Device breakdown (40%)
- Interconnect melt-down (30%)
- Cross-domain ESD issues (15%)
- ESD Network (10%)
- misc (5%)
- Cross Domain (10%)

ESD failures impact first silicon success
Device Breakdown

Why is it more important now?

ESD Design window from 130 nm to 32 nm technology

What are the common causes for such failures?

# Signal bus R check
BEGIN_ESD_RULE
NAME sigbump2diode_Rcheck
TYPE BUMP2CLAMP
ARC_R 0.1
TERMINAL_NET_GROUP SIGNAL
CLAMP_TYPE1 D1 D2
END_ESD_RULE

# Power Bus R Check
BEGIN_ESD_RULE
NAME Pwr_Bus_R_check
TYPE CLAMP2CLAMP
ARC_R 0.1
TERMINAL_NET_GROUP POWER GROUND
FROM_CLAMP_TYPE D1 D2
TO_CLAMP_TYPE PWRCLMP
END_ESD_RULE

# Power2Ground R check
BEGIN_ESD_RULE
NAME PWR2GND_R_check
TYPE BUMP2BUMP
LOOP_R 5
PARALLEL_R 1
TERMINAL_NET_GROUP POWER GROUND
CLAMP_TYPE PWRCLMP
SHORT_BUMP_IN_NET_GROUP POWER GROUND
END_ESD_RULE

How can PathFinder help?
**Device Breakdown**

**Case Study: Machine Model Failure**

R1+R3>>R1+R2 causing device breakdown

R1+R3>2ohms, why?

Short Path Trace (SPT) debug in Pathfinder

Missing VIA7 causes long scenic route from bump to D1 as shown in Short Path Trace (SPT)

Why is SPT showing scenic route??
Interconnect Melt-down

Why is it more important now?

What are the common causes for such failures?

Current crowding on ESD device
Insufficient via-cuts/ineffective clamps
Insufficient wire width on ESD pathways

Positive Zap

Negative Zap

Technology vs Interconnect Current limits

Current density vs technology node

Process Technology (nm)

ESD Current Density (mA/μm)

0 50 100 150 200 250 300 350 400 450

ESD Current Density (mA/μm)

0 40 80 120 160

Why is it more important now?

What are the common causes for such failures?
Interconnect Melt-down

How can PathFinder help?

Signal Bus CD checks

Power/Ground Bus CD checks

Power2Ground CD checks

Define Interconnect CD limits

- $M_x = x \text{ mA/um}$
- $M_y = y \text{ mA/um}$
- $M_z = z \text{ mA/um}$
- $RDL = r \text{ mA/um}$

# Signal bus CD check
BEGIN_ESD_RULE
NAME signal_bump2diode_CD_check
TYPE CD
ZAP_CURRENT 1.3A # ~2kV HBM zap
B2C_NET_GROUP SIGNAL
SHOTGUN_MODE 1
END_ESD_RULE

# Power Bus CD Check
BEGIN_ESD_RULE
NAME Pwr_Bus_CD_check
TYPE CD
ZAP_CURRENT 1.3A # ~2kV HBM Zap
C2C_NET_GROUP POWER GROUND
FROM_CLAMP_TYPE D1 D2
TO_CLAMP_TYPE PWRCLMP
END_ESD_RULE

# Power2Ground CD check
BEGIN_ESD_RULE
NAME PWR2GND_CD_check
TYPE BUMP2BUMP
ZAP_CURRENT 1.3A # ~2kV HBM Zap
TERMINAL_NET_GROUP POWER GROUND
CLAMP_TYPE PWRCLMP
SHORT_BUMP_IN_NET_GROUP POWER GROUND
END_ESD_RULE

# Clamp IV Model
BEGIN_CLAMP_IV
NAME <I-V_clamp_name>
Ron <Ron+> [<Ron-]>
VT1 <VT1+> [<VT1-]>
VH <VH+> [<VH-]>
ROFF <ROff+> [<ROff-]>
END_CLAMP_IV
One finger of D1 was damaged during +ve HBM Zap

Case Study: 2KV HBM Failure

PathFinder Current Density Map

Current Crowding in Diodes
- Poor Connection of diode fingers
- Missing Via from metal8 to metal6
Cross-domain ESD Issues

Why is it more important now?

What are the common causes for such failures?

Unintentional ESD discharge path

Intentional ESD discharge path

Insufficient/unconnected bridge diodes

High Ground bus R

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Cross-domain ESD Issues

How can PathFinder help?

# Clamp connectivity Checks in PathFinder
TCL> perform clampcheck
   # pin2pin connectivity
   \-allNetConn
   # report disconnected net pairs
   \-rptDisconn

# Signal bus CD check
BEGIN_ESD_RULE
NAME VSS_Bus_R_Check
TYPE C2C
FROM_CLAMP_TYPE PWRCLMP
TO_CLAMP_TYPE B2B_DIODE
ARC_R 0.5
END_ESD_RULE

#Cross-domain CD Check
BEGIN_ESD_RULE
NAME Cross_domain_CD_Check
TYPE CD
ZAP_CURRENT 1.3A #~2kV HBM Zap
NET_PAIR VDD1 VSS2
END_ESD_RULE

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Cross-domain ESD Issues

Case Study: IP Integration Issue

- Global VSS connection having ~170um wire with 18.5ohms of resistance
- Ineffective B2B diode near the PLLVSS bump
  ➔ Missing connection in higher metal layers

5ohms of G2G R, Why?

Short Path Trace (SPT) debug in PathFinder
Ground2Ground connections (during IP integration) is a common cause for ESD failure.

Missing metal9 connection b/w SOC and IP for VSS

0.4um M9 strap causing 40x CD violation

Cross-domain ESD Issues

Case Study: IP Integration Issue

Current parallel to wire direction at query position: 3.8 A

Half node scale: 0.9

EM mode: peak

EM rule: const based (EMCurrentDensity: 0.27144 A/um, width: 0.347127 um)

EM percentage: 4032.94% (EM current limit: 0.0942242 A)
PathFinder Core Technologies & Benefits

**Capacity**
- Full-chip capacity with package impact

**Accuracy**
- ESD snap-back device modeling
- Current crowding on diode fingers
- IV curve support

**Usability**
- Rich GUI for debug and optimization
- Root-cause the bottleneck in ESD bus
ESD-aware SoC Design Flow

- **IO ring ESD bus planning**
  - Signal IO
  - IO Power Clamps
  - Bridge diodes

- **Analysis driven clamp placement**
  - ESD Clamp

- **Resistance and current density limit sign-off**
  - GPIO (VDDG)
  - CPU CORE (VDDC)
  - Memory/Cache (VDDM)

**Floor plan**

- **IO Pad level**
- **IO Ring IP level**
- **Final sign-off**
Summary

• Full chip-level ESD integrity analysis solution

• PathFinder coverage:
  – Layout connectivity checks
  – Resistance checks
  – Interconnect failure checks
  – Dynamic CDM checks for IPs

• Part of ESDA reference flow and TSMC reference flow